Graph Based Analytical Approach for Evaluation of Semi Markov Process Model for System-on-Chip Communication

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Abstract

While number of components on a system-on-chip increase, on-chip communication becomes diverse and complex. To cope with this complexity during design space exploration, designers raise modeling abstraction to system level. Careful design space exploration of communication architecture is necessary not only to meet hard/soft performance constraints, but also to conceive optimum design within design time deadlines. Moreover, plethora of choices available for communication architecture results in larger design space. Thus, quick estimation of performance of communication architecture is imperative at all abstraction levels. This paper presents efficient approaches for performance evaluation, one of which is based on hierarchical concurrent flow graph (HCFG) approach. The analytical formulation is based on Semi Markov Process (SMP) model for a Processing Element (PE) mapped to (i) a single shared bus architecture and (ii) hierarchical bus bridge architecture. In particular, we focus on building model for single shared bus architecture and extend the approach to model architecture consisting of hierarchical buses connected through bus bridge. Our modeling approach provides early evaluation of performance parameters viz. memory bandwidth, PE utilization, average queue length at memory and average waiting time seen by a PE. We report results of evaluating performance metrics using analytical approaches - (i) first, based on Analytical Formulation of Model Equations (AFOME) [1] [2] and the other, (ii) Hierarchical Concurrent Flow Graph based approach [3]. Proposed analytical approach using HCFG is not only time efficient, but also provides detailed stochastic properties of performance parameters, as compared to simulation. We validate the results by performing Monte Carlo simulation. Both approaches are time efficient as compared to the Monte Carlo simulation of the same underlying model.

I. Introduction

Ever increasing functionality of the systems in diverse and emerging applications like telecommunications and multimedia makes System on Chip (SoC) design complex. Furthermore, stringent time and performance requirements imposed upon them impede challenges to the designers. To respect higher performance of such systems, designer integrates number of concurrent processing

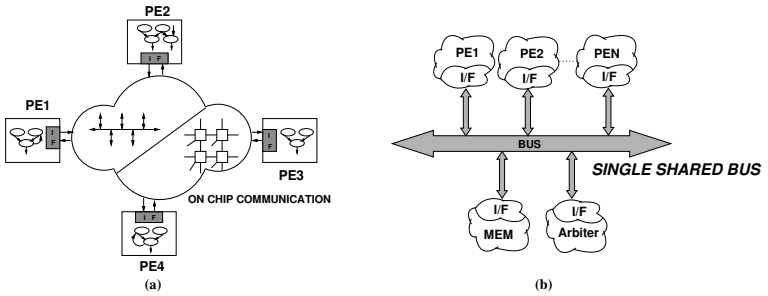

Fig. 1. (a) Generalized SoC architecture and (b) Single shared bus communication architecture.

elements (PEs)/intellectual property (IP) blocks in single SoC. Reuse of pre-designed and pre-verified hardware/software IPs is the way to manage increased complexity and time deadlines of SoCs. An SoC performs two orthogonal aspects of system functionality: computation and communication [4] [5]. System computation task is mapped to heterogeneous PEs/IPs, while communication architecture performs communication between PEs/IPs. Generalized SoC architecture comprising PEs and communication architecture is depicted in Fig. 1(a). Now-a-days fully optimized IPs are available. In SoCs, integration of optimized IPs through suitable communication architecture in short time is desirable. But, it requires full understanding of functionality and interfaces of each IPs. Moreover, no single tool supports seamless modeling and simulation of heterogeneous PEs/IPs with their communication. Integration of pre-verified IPs may not meet communication requirements of entire system, if designer underestimates communication architecture exploration. It includes selection of topology, mapping of communication requirement to selected topology and selection of appropriate protocol. At each stage of exploration, quick performance estimation becomes imperative. This has been motivation for our efforts for estimating performance of communication architecture at system level.

In this paper, we propose an analytical approach based on Semi Markov Process (SMP), for performance estimation of bus based communication architectures. First, we propose semi Markov model for Single Shared Bus (SSB) architecture, which we enhance for the modeling of Hierarchical Bus (HB) architecture. In case of both the architectures, we employ Hierarchical Concurrent Flow Graph (HCFG) based analytical analysis tool for performance evaluation of SMP model. In next section, we present brief background of SMP and HCFG, and review of performance estimation techniques proposed in literature. We develop modeling framework and performance evaluation for SSB architecture in Section III. Section IV gives modeling extension to deal with HB architecture. In Section V, we present results. We conclude in Section VI.

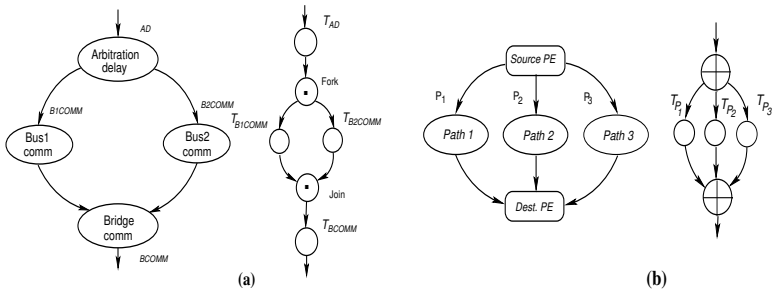

Fig. 2. (a) Communication with (a) AND concurrency, (b) OR concurrency,

II. Background

Communication architecture allows exchange of data and control signals between various system components. Variety of communication architectures are- bus-based, network-on-chip (NoC) based [6], hybrid bus-NoC architectures [7], cross-bar architecture [8] and multiple bus architecture [9]. Bus based architectures have different variants including dedicated buses, SSB and network of shared buses. In SoCs and embedded applications bus based architectures are popular because these are simple, consume less power and area. Moreover, bus based architectures not only meet demands of communication but also end up with cheaper design in low end and high volume applications. Besides, commercial architectures such as AMBA from ARM, CoreConnect from IBM are being widely used as infrastructure IPs. So, we have chosen bus based architectures for modeling.

A. Semi Markov Process

Semi Markov process is a stochastic process which makes transitions from state to state in accordance with the Markov chain. The amount of time SMP spends in each state before making transition is a random variable. This time is called sojourn time. We express it in terms of clock cycles for which a PE computes, communicates or waits for communication. Mean value of sojourn time in state i is denoted by η_i.

B. Hierarchical Concurrent Flow Graph Approach

Hierarchical concurrent flow graph is an approach for performance evaluation of concurrent and hierarchical design flow graph. Previously, this analysis tool has been used for evaluation and improvement [3] of process completion time of VLSI design processes. Our work utilizes the same approach for evaluating performance metrics of communication architectures. An SoC communication is hierarchical and concurrent e.g. communication on BUS1 and BUS2 of Fig.4 in Section IV. Hierarchy provides efficient communication between PEs/IPs with varying bandwidth. Besides, two inherent concurrencies are present in HB architecture. Since both communications over BUS1 and BUS2 (Fig.4) must be completed before initiating communication across bus bridge, this type of

concurrency is called AND concurrency. Two special "operation" nodes are included in the communication graph for AND-concurrency as shown in Fig. 2(a). These nodes are labeled $\odot$ and are special operation nodes with no weights associated with them. The operation node with in-degree one is called as "fork" node whereas the operation node with out-degree one is referred as "join" node.

Another form of concurrency prevalent in NoC architectures is OR concurrency, where communication architecture attempts to transfer data from source PE to destination PE through alternate communication paths. Different possible paths depend on routing algorithms used. Communication graph for OR concurrency is shown in Fig 2(b). Two special nodes, called OR-operation nodes, are included to describe OR-concurrency in the communication flow graph. The nodes are labeled $\oplus$ and are referred to as "fork" and "join" nodes. The operation nodes are not associated with node weights. We will represent SMP model of the communication architecture under consideration with HCFG equivalent. Nodes in HCFG correspond to various states of SMP model of a PE viz. computing, accessing, full waiting or residual waiting. The weight of the nodes corresponds to mean sojourn time of respective state. Directed edges represent communication scheduling information of a PE and influence of other PEs.

C. Related Work and Our Contribution

Many approaches for performance evaluation of on chip communication architecture have been proposed in literature: Simulation approach uses communication models at various levels of abstraction. Work in [10] presents simulation by abstracting the system at cycle count accurate at transaction boundaries. [11] proposes formal concurrent modeling approach based on operation state machine for entire system comprising of computation and communication together. Analytical approach [12] estimates communication overhead in the pipelined communication path. They consider impact of various protocol parameters such as burst size and frequencies on variation of data transfer. S. Dey and S. Bommu in [13] introduces worst case static performance analysis of the system comprising concurrent communicating processes. Estimation reveals significant underestimate if synchronization overhead is not accounted. Two phase hybrid approach encompasses both simulation and analytical approaches [14] [15] to exploit benefits of both. [15] performs initial co-simulation with the abstracted communication in the first phase. Time inaccurate communication analysis graph is analytically analyzed in the second phase by specifying communication architecture. Queueing analysis in [14] uses analytical approach to prune the design space and then entire system simulation of the selected architectures.

Main contribution of the paper is system level analytical framework for performance estimation of communication architecture based on SMP. Our focus is on bus based single shared bus architecture, and its extension to hierarchical buses connected by bus bridge. Our modeling approach provides estimation of performance parameters viz. estimation of bandwidth (BW), PE utilization (PU), average queue length ($\overline{L}$) at memory and average waiting time ($\overline{W}$) seen by a PE. The input parameters to the model are number of PEs (N), the mean think time

of PE ($\overline{T}$), the mean connection time between PE and memory ($\overline{C}$) and second moment of the connection time ($\overline{C^2}$). Similar approaches have been considered in past [8] reports an approach for cross bar bus architecture whereas [9] reports an approach for multiple bus architecture. Work in [9] uses two stage arbitration for shared memory modules and buses. [8] employs only one stage arbitration for the shared memories. Our approach differs in communication architecture and bus arbitration. Since the communication behavior of a SSB and HB architectures is quite different from that of the multiple bus and the crossbar architectures, however, their approach cannot be directly applicable. Instead, we make several changes to model SSB and HB architectures. We consider single bus arbitration for SSB architecture and two-stage bus arbitration for HB architecture. Further our work uses HCFG based evaluation approach reported in V. Sahula's work [3] which not only provides stochastic properties of performance parameters but also very efficient as compared to simulation. We employ HCFG analytical approach for performance evaluation of SMP models for SSB and HB architectures.

III. Proposed SMP Model Formulation For SSB Architecture

We develop the semi Markov model for a SSB architecture in this section. We adopt basic idea and the notations from [9] and propose SMP based modeling approach for a SSB architecture. Synchronous SSB architecture consisting of N processing elements, PE_1, PE_2,...,PE_N competing for the use of a bus is depicted in Fig. 1(b). Arbiter of N-user one-server type resolves the bus access conflict. Characteristic behavior of each PE is assumed to be independent and statistically identical and thus modeling of one PE is sufficient for performance estimation of the entire system [9].

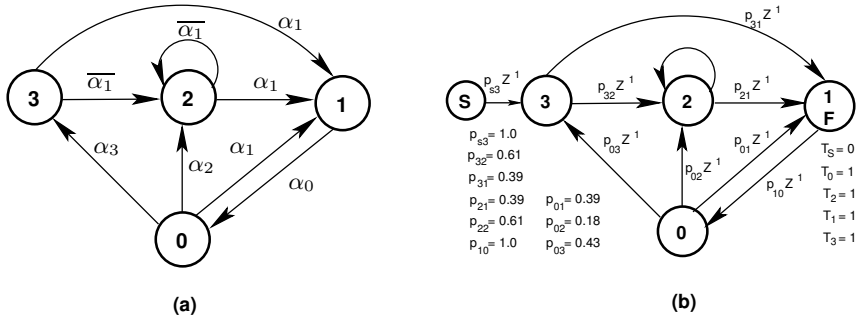

Fig. 3. (a) semi Markov model for SSB architecture and (b) HCFG of SSB architecture with N=2.

Semi Markov model of a PE is shown in Fig. 3(a) and has four states state 0- $thinking$, state 1- $accessing$, state 2- $full\ waiting$ and state 3- $residual\ waiting$. In each respective state model spends average time η_0, η_1, η_2 and η_3 called sojourn time before making transition.

When a PE performs computation, the situation is modeled as $state$-0. The process leaves $state$-0, whenever a PE generates a request and enters either in $state$-1 or 2 or 3, depending upon memory status (idle or busy) and arbitration.

Process enters the $state$-1, if memory is idle and a PE wins arbitration. The process enters the $state$-2, if memory is idle, but a PE does not win the bus arbitration. From $state$-2, after η_2 time, if pending request wins arbitration, the SMP enters to $state$-1, otherwise it remains in $state$-2. The process enters the $state$-3, if bus is busy, at the time of request. From $state$-3, after η_3 time, process either enters the $state$-1 if access is granted or it enters the $state$-2 if fails to get access. From $state$-1 the process always returns to $state$-0. Performance metrics from steady state probabilities of model are computed using Analytical Formulation of Model Equations (AFOME) approach [1] [2] in terms of model input parameters $\overline{T}$, $\overline{C}$, $\overline{C^2}$ and N.

A. SMP Model Evaluation Based on HCFG Approach

In this section, we explain the HCFG methodology used for computing performance parameters for SSB architecture. For this, we construct hierarchical concurrent flow graph G from SMP model of a single shared bus as follows. We add one extra node I that represent the initial task, with zero communication time. We draw directed edge (I, x), in G, where x is a state of SMP with zero in-degree [3]. In our case, we chose minimum in-degree. So, residual waiting state ($state$-3) is taken as x state for SMP model of SSB. Transition probability of the edge (I, x) is taken as one. Next, we map average sojourn times of the states of SMP to the task execution times of corresponding nodes of HCFG, T_js. Transition probabilities of SMP, are correlated to the weight p_{ij} of an edge (i, j) of HCFG.

To compute limiting probabilities of all states we consider one state at a time as a final state denoted by F and assign $T_j = 1$, $j = 0, 1, 2, 3$, $T_s = 0$. In Fig. 3(b), we show a HCFG for computing steady state probability of accessing $state$-1 of SSB architecture, when two PEs are mapped. Textual description of HCFG is executed to obtain limiting probability of the state. Thus, we compute steady state probabilities, $P_0 - P_3$ of all the states of the SMP model with varying number of PEs from one to eight. We compute performance metrics in term of steady state probabilities as follows:

$$BW = N\,P_1 \qquad PU = P_0 + P_1$$
$$\overline{L} = N\,(P_2 + P_3) \qquad \overline{W} = (\eta_2\,\alpha_2 + \eta_3\,\alpha_3)/\alpha_1$$

IV. Model Extension for Hierarchical Bus Using Bus Bridge

In this section, we propose extension of semi Markov model of SSB architecture discussed in previous section to deal with hierarchical buses connected by bus bridge. Let us consider, HB architecture consist of two shared buses BUS1 and BUS2 connected by bus bridge as shown in Fig. 4. Each bus has N processing elements PE_1, PE_2,...,PE_N competing for the use of shared buses to access shared memories MEM1 and MEM2. We refer parameters of BUS1 as local parameters, and parameters of BUS2 as global parameters. In HB architecture framework, behavior of each PE is influenced by local as well as global PEs. Each PE can generate two requests. X_l -probability of local request, in which only local bus BUS1 would be used to access local memory MEM1 by

one of the local PE. X_g -probability of global request in which both buses would be used to access global memory MEM2 by one of the local PE. In first case, arbitration of local bus is sufficient while in second case two stage arbitration of local and global bus is essential. Zero arbitration delay is assumed in both cases.

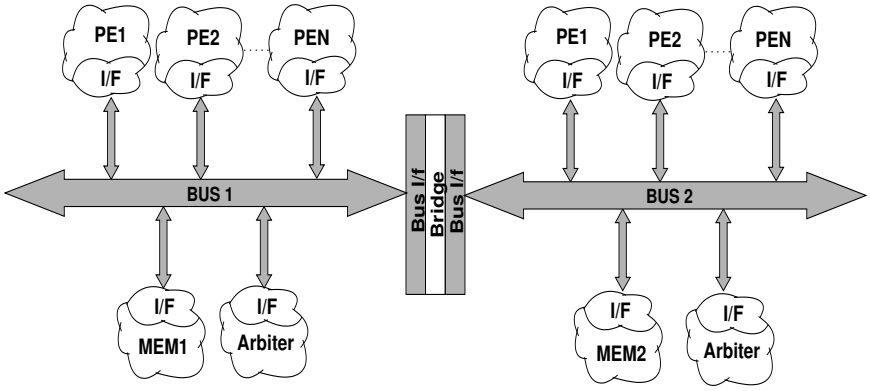

Fig. 4. Hierarchical bus architecture.

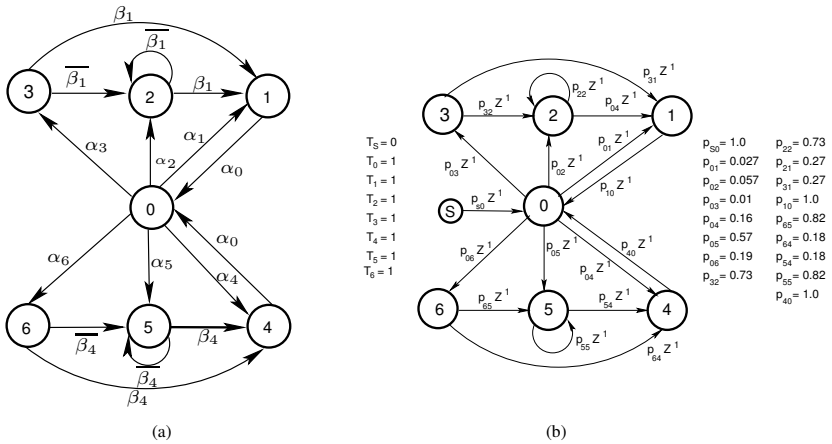

Fig. 5. (a) SMP Model and (b) its HCFG Representation, of a PE of HB architecture.

Semi Markov process model of a PE is depicted as in Fig. 5(a). SMP has seven states. $State$-1, $state$-2 and $state$-3 are correspond to local memory similar to the model of a PE of SSB architecture , we call these as local accessing, local full waiting and local residual waiting states respectively. States correspond to global memory namely, $state$-4, $state$-5 and $state$-6 are refereed as global accessing, global full waiting and global residual waiting states respectively. Think state,

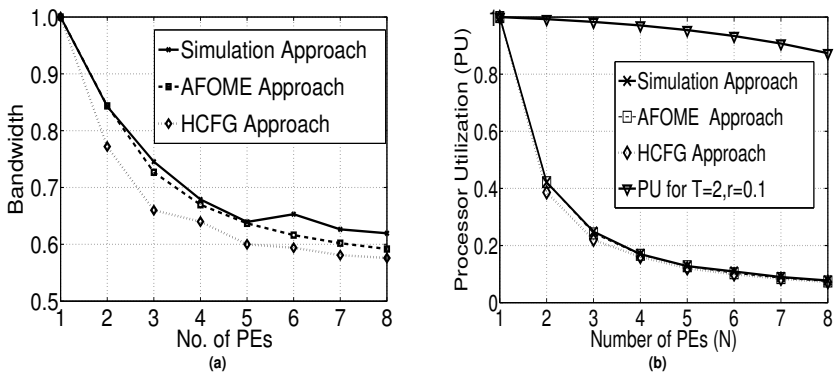

Fig. 6. Variation of (a) BW, (b) PU with N for SSB architecture.

$state$-0 is similar as previous. Steady state probabilities and performance metrics of the model are derived using AFOME approach [1] [2].

A. SMP Model Evaluation Using HCFG

As discussed in Section III, we construct HCFG for HB architecture from SMP model. Fig. 5(b) shows a HCFG graph for computing steady state probability of local accessing $state$-1 for local requesting probability $X_l = 0.1$. Computing state ($state$-0) is now taken as x state. We map average sojourn time of the states and transition probabilities of SMP to HCFG. We consider one state as a final state F at a time and compute its steady state probability. For this we assign $T_j = 1$, $j = 0, 1, 2, 3, 4, 5, 6$, $T_s = 0$ and execute textual description of HCFG . Thus, steady state probabilities, $P_0 - P_6$ of all the states of the SMP model with varying X_l from 0.1 to 0.9 are obtained. Performance metrics for local memory and global memory are computed from steady state probabilities. These are expressed as follows:

$$BW_l = N\,P_1 \qquad BW_g = N\,P_4$$
$$\overline{L_l} = N\,(P_2 + P_3) \qquad \overline{L_g} = N\,(P_5 + P_6)$$
$$\overline{W_l} = \eta_2(\alpha_2 + \alpha_3\overline{\beta_1})/\beta_1 + \eta_3\alpha_3 \qquad \overline{W_g} = \eta_5(\alpha_5 + \alpha_6\overline{\beta_4})/\beta_4 + \eta_6\alpha_6$$

V. Results

We have estimated performance parameters of SMP based models of SSB and HB architectures by applying two analytical approaches-AFOME [1] [2] and HCFG approach, and simulation approach. In this section, we present performance evaluation results of one example each for SSB and HB architecture. Results are compared with simulation results of SMP models. The simulation was performed using SIMULINK on P-IV, 1 GB Linux-WS.

As first example, a multiprocessor (PEs) system having a SSB architecture is evaluated and various performance parameters are obtained using the approaches discussed in Section III. Various model input parameters are assigned values as

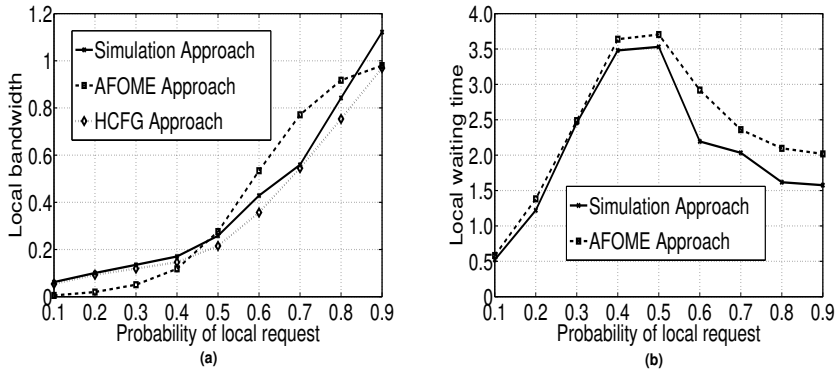

Fig. 7. Effect of X_l on (a) BW_l, (b) $\overline{W_l}$ for HB architecture.

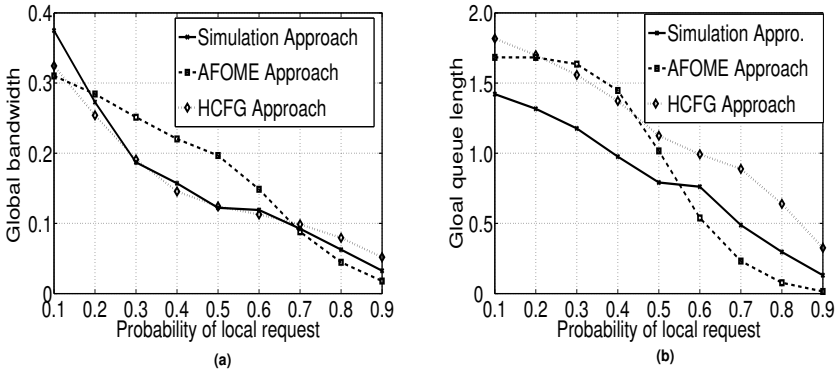

Fig. 8. Variation of (a) BW_g and (b) $\overline{L_g}$ for HB architecture.

follows- $\overline{C} = 2$ cycles, $\overline{T} = 0$ cycles, coefficient of variation of $\overline{C}, C_v = 0$ (where $C_v = (\overline{C^2}/(\overline{C})^2 - 1)^{1/2}$). We varied number of PEs from one to eight. In Fig. 6(a), effect of variation of number of PEs on BW is shown with proposed approaches as well as simulation approach. Reduction in bandwidth from 1 to 0.59 is observed from the Fig. 6(a) as number of PEs mapped to SSB architecture are increased from one to eight. For multiple PEs (N=8), our results are similar to the results in [9] under the assumption that re-submitting pending request in waiting state is considered. If single PE is mapped to the bus, we obtain parameter values as: BW=1, PU=1, $\overline{L}$ =0 and $\overline{W}$ =0. This case refers to dedicated bus and signifies that communication always takes place if sender and receiver are ready without waiting time or contention.

In Fig. 6(b), a plot of variation of processor utilization against number of PEs is shown. As observed from the Fig. 6(b), processor utilization becomes poorer from 1 to 0.073 if number of PEs mapped to SSB architecture are varied from

one to eight. This is intuitive as mapping a large number of processors to the bus implies that they spend more time in waiting states 2 and 3 for the bus to become free. Although, degradation is not significant in computational intensive applications. To justify this hypothesis, we incorporate additional input parameter to the SMP model of SSB architecture, probability of request r generated by a PE. We take equal number clock cycles for computation and communication i.e. $\overline{C}$=$\overline{T}$=2 cycles, remaining parameters are same as that of previous example. Typical value of bus request rate in multimedia applications is 11.5% [14]. So, we chose r =0.1, means that 10% of the total execution time is used for communication. Processor utilization of this experiment is shown in Fig. 6(b). It indicates degradation in processor utilization is from 1 to 0.87 i.e. only 13% as compared with 93% of previous case. Queue length at memory and waiting time seen by a PE as expected, increases with increase in N.(Figs. are not shown).

In second example, performance metrics of a PE mapped to the HB architecture were estimated with variation of probabilities of local request X_l and global request X_g by applying three approaches. Input parameters are taken as $\overline{C_l} = 2$ cycles, $\overline{C_g} = 2$ cycles and $N = 2$. Remaining parameters are same as that of previous example.

Results showing variation of BW_l with X_l = 0.1 to 0.9 is reported in Fig. 7(a). It shows, BW_l increases with X_l, with small boost in the beginning because, probability of global request is higher than local request and global request has higher priority than local request. Rate of increase is more beyond $X_l = 0.4$. Fig. 8(a) shows, variation of BW_g with X_l = 0.1 to 0.9. It also indicates increase in global bandwidth with global requesting probability. But, maximum local bandwidth is 0.97 while maximum global bandwidth is 0.31 as observed from figures 7(a) and 8(a).

This is because two stage arbitration for BUS1 and BUS2 is essential for accessing global memory, so a PE requesting for global memory has to wait in local as well as global waiting states and wins arbitration of both buses when both would become free. This infers that PE having higher communicating payload with memory should be mapped to the same bus as that of memory to achieve better performance similar to the explanation given in [15]. Thus designer could find optimum mapping early in design cycle.

Fig. 7(b) indicates that local waiting time increases upto $X_l = 0.4$ as global request are dominating and then decline rapidly. Similar observation can be noted for global waiting time with global requesting probability X_g. But, global request has to wait more time as compared to local request even if requesting probabilities are same. For example local wait time is 2.01 units for X_l=0.9, while global wait time is 10.85 units for X_g=0.9. Fig. 8(b) indicate increase in global queue length with X_g.

Execution time and average error of HCFG approach are compared with simulation in the Table I.

VI. Conclusions And Future Work

This paper presents SMP based modeling approach for SSB and HB architectures. We have evaluated performance metric viz. bandwidth, processor

TABLE I
EFFECTIVENESS OF HCFG APPROACH

Parameter	**BW**	**PU**	$\overline{L}$	$\overline{W}$
% Average error (Abs.)	4.68	4.68	21.88	12.78
Execution Time (second)	**Proposed**		**Simulation**	
	0.0065		884.16	

utilization, queue length and waiting time with number of processing elements for SSB architecture. For HB architecture performance parameters for local and global memories are evaluated with local or global requesting probabilities. Results obtained with HCFG evaluation approach are validated using simulation. Proposed approach took much less time as compared with simulation as well as equally accurate as that of simulation. HCFG technique provides not only fast evaluation but also gives probability distribution quickly. Our future work will focus on further model extension based on interactive semi Markov process to cope with inherent communication concurrency.

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