Generalized Semi Markov Process Model for Hierarchical Bus Bridge based SoC Communication Architecture

Abstract— **The modern-day System-on-Chip communication has following complex characteristics- (a) the communication times of individual transaction are difficult to predict, (b) concurrent communication techniques are employed to meet the performance of emerging applications, and (c) communication is hierarchical. Thus, performance of communication architecture plays major role in the performance of the system. An early and efficient performance estimation of communication architecture is essential to select appropriate communication architecture from the possible choices within design time deadlines. In this paper, we propose an analytical performance estimation of hierarchical bus bridge communication architecture, based on generalized semi Markov process model. Our modeling approach provides early estimation of performance parameters viz. memory bandwidth, average queue length at memory and average waiting time seen by a processing element. The input parameters to the model are number of processing elements, the mean computation time of processing element and the first and second moments of connection times between the processing element and memories. We validate efficacy of modeling approach by comparing the results against those obtained by Monte Carlo simulation for the same underlying model.**

I. Introduction

Due to continuous development in manufacturing technology, global interconnect delay becomes major performance bottleneck in Deep Sub-Micron (DSM) System-on-Chip (SoC) design [1]. As a consequence, communication architecture emerges as one of the significant performance determining component of SoC, which provides mechanism for integrating heterogeneous system components viz. CPUs, DSPs, ASIP, memories, custom hardware etc. Thus, to meet performance requirement of SoC as a whole, selection of appropriate communication architecture and its customization play a key role in SoC design. Furthermore, availability of several commercial communication architecture such as, AMBA and IBM CoreConnect for SoCs provides designer with variety of design alternatives. Therefore, an efficient performance estimation technique is essential for selection of optimum communication architecture from a wide design space within design time deadline.

Different types of communication architectures have been used for integrating system components viz. bus-based, network-on-chip (NoC) based, hybrid bus-NoC architectures, cross-bar architecture and multiple bus architecture. Bus based architectures are further classified as dedicated buses, single shared bus and network of shared buses. In SoCs and embedded applications bus based architectures are popular because these are simple, consume less power and area. Moreover, performance of bus based architectures not only suffices for low end and high volume applications but also results in cheaper design.

Communication architecture, which we consider in this paper, is composed of two shared buses BUS1 and BUS2, and connected by a bus bridge as shown in Fig. 1. Here, N number of Processing Elements (PEs) on each bus, compete to access shared memories MEM1 or MEM2. Our formulation is based on shared memory communication model in which SoC function involves communication of one of the PEs with one of the memories.

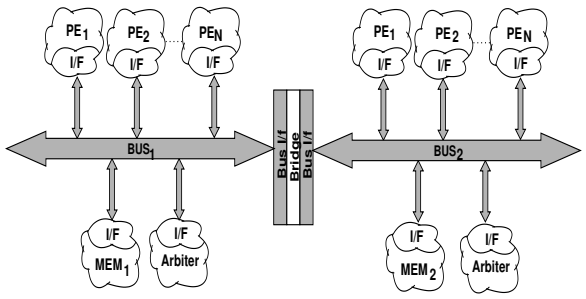

Fig. 1. Hierarchical bus bridge communication architecture.

In this paper, we propose performance estimation method based on Generalized Semi Markov Process (GSMP) model for Hierarchical Bus Bridge (HBB) communication architecture. The approach has been proposed as an extension to the performance estimation of a single shared bus communication architecture [2] [3]. In Section II, we present background and previous work of performance estimation techniques. Section III, contains discussion on performance estimation framework for HBB architecture. We present the results in Section **??** and conclude in Section V.

II. Related Work and paper contribution

A. Related Work

Many approaches for synthesis and performance evaluation of on chip communication architecture have been proposed in the literature. Work reported in [4], uses static performance estimation technique for allocation of communication units or channels. Authors in [5] employ semi Markov process model for estimating performance of multibus communication architecture. In our work [2] [3], we propose GSMP model

for an efficient performance evaluation of a single shared bus communication architecture. Analytical approach as in [6] estimates communication overhead in the pipelined communication path. The work considers impact of various protocol parameters such as burst size and frequencies on variation of data transfer. Simulation approach uses communication models at various abstraction levels. Work in [7] proposes formal concurrent modeling approach based on operation state machine for entire system comprising of computation and communication. Two phase hybrid performance estimation approach has been proposed in [8]. Authors in [8] perform initial co-simulation with the abstracted communication in the first phase. Time inaccurate communication analysis graph is analyzed in the second phase by specifying communication architecture.

B. Contribution of the paper

Main contribution of the paper lies in the proposal for system level analytical framework for performance estimation of HBB communication architecture. The formulation is based on GSMP model of communication architecture. The approach has been presented as an extension to the performance estimation of a single shared bus communication architecture [2] [3].

Our modeling approach provides estimation of separate performance parameters for local and global memory. For local memory we estimate- local bandwidth (BW_ℓ), local average queue length at memory ($\overline{L_\ell}$) and local average waiting time seen by a PE ($\overline{W_\ell}$); whereas in case of global memory, we estimate- global memory bandwidth (BW_g), global average queue length at memory ($\overline{L_g}$) and global average waiting time seen by a PE ($\overline{W_g}$). The input parameters to the model are number of PEs (N), the mean think time of PE ($\overline{T}$), first and second moment of local connection time between PE and memory ($\overline{C_\ell}$, $\overline{C_\ell{}^2}$) and first and second moment of global connection time between PE and memory ($\overline{C_g}$, $\overline{C_g{}^2}$).

III. GSMP model for HBB architecture

A. Generalized semi Markov process

Generalized semi Markov process, is a stochastic process which makes transitions from state to state in accordance with the Markov chain where amount of time spent in each state before making transition, is a random variable called sojourn time. In short, an GSMP has state space {1,2,.....K} and it can be in any one of them. Each time it enters in state *i* ($1 < i < K$) and spends mean sojourn time η_i, before making transition to *state j* with probability p_{ij}.

B. Model Formulation

In this section, we proposed extension of GSMP model of single shared bus architecture [2] [3] to HBB architecture of Fig. 1. Let us consider HBB architecture of Fig. 1. All PEs are assumed to be identical and hence GSMP model of a PE suffices for functional modeling. For brevity, let us consider a scenario when a PE mapped to BUS1 generates a request to access either MEM1 or MEM2. With reference to this PE connected to BUS1, parameters of MEM1 and MEM2 are referred to as local and global parameters, respectively.

In HBB architecture, each PE can generate two requests. Let X_ℓ be the probability of local request, implying only BUS1 would be used to access MEM1 and arbitration of BUS1 is sufficient. Whereas, let X_g be the probability of global request where both BUS1 and BUS2 would be used to access MEM2 and two stage arbitration of BUS1 and BUS2 is essential. GSMP model of a PE in aforementioned scenario is depicted in Fig. 2. Local accessing state labelled as *State 1*, local full waiting state labelled as *state 2* and local residual waiting state labelled as *state 3* correspond to MEM1. State *state 4*, *state 5* and *state 6* are analogous states when a PE attempts to access MEM2. These are respectively referred as global accessing state, global full waiting state and global residual waiting state.

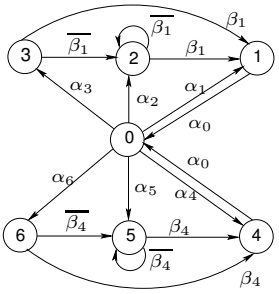

Fig. 2. GSMP model of a PE in HBB architecture

Transition from *state 0* to *state 1* takes place, when MEM1 and BUS1 both are idle with the probability $(1 - BUSY)^2$ and request wins arbitration with the probability WIN. Alternatively, GSMP transits from *state 0* to *state 2* when MEM1 and BUS1 are idle and local request does not win arbitration with the probability $(1 - WIN)$. Similarly, GSMP makes transition from *state 0* to *state 3* if at the time of request either (i) MEM1 is busy or (ii) MEM1 is idle but BUS1 is being used by PEs mapped to BUS2. Pending local requests of *state 2* and *state 3* are reconsidered after elapse their mean sojourn times and (a) if granted access, a PE enters to *state 1*, (b) otherwise it enters in the *state 2*. GSMP transits from *state 0* to *state 4* when BUS1, BUS2 and MEM2 are idle and, global request wins arbitration of BUS1 and BUS2. Alternatively, GSMP transits from *state 0* to *state 5* when MEM2, BUS1 and BUS2 are idle, but global request does not win arbitration of either BUS1 or BUS2. It enters *state 6*, if either (i) MEM2 is busy or (ii) MEM2 is idle and either of BUS1 and BUS2 is busy. Pending global requests of *state 5* and *state 6* are reconsidered after elapse their mean sojourn times and (a) if granted access, a PE enters to *state 4*, (b) otherwise it enters in the *state 5*. From *state 1* and , *state 4* the process always returns to *state 0*.

C. Analytical Formulation of Model Equations

In this section, we present Analytical Formulation of Model Equations (AFOME) to evaluate the performance metrics of

HBB architecture. Local request gets access to a local memory, when model of a PE transits from *state 0* or *state 2* or *state 3* to *state 1*. Similarly, a PE accesses a global memory when transition from *state 0* or *state 5* or *state 6* to *state 4* takes place. Let R_l and R_g are the probabilities that a request gets access to local and global memory at the beginning of bus cycle written as follows:

$$\begin{aligned} R_l &= X_l\mu_0 + \mu_2 + \mu_3 \\ R_g &= X_g\mu_0 + \mu_5 + \mu_6 \end{aligned} \quad (1)$$

where $\mu_k, k \in \{ 0,2,3,5,6 \}$ is the probability of leaving k^{th} state to gain corresponding accessing state.

The average sojourn times of different states of the model are obtained from following discussion. (i) For *state 0*, *state 1* and *state 4* ηs are nothing but mean computation time, mean local communication time and mean global communication time. (ii) In case of *state 2*, η is obtained from local and global communication time. Local request of a PE under consideration waits in state *state 2* when any other local or global request wins the arbitration. (iii) For *state 5*, if any other global request wins arbitration, global request of a PE under consideration waits in *state 5*. (iv) For *state 3* and for *state 6*, ηs are obtained from residual times of *state 1* and *state 4*. Thus, average sojourn times of different states of the model are given in equation (2).

$$\eta_j = \begin{cases} \overline{T} & j = 0 \\ \overline{C_l} & j = 1 \\ \overline{C_g} & j = 4 \\ \frac{R_l\,\overline{C_l} + R_g\,\overline{C_g}}{R_l + R_g} & j = 2 \\ \frac{R_g\,\overline{C_g}}{R_g} = \overline{C_g} & j = 5 \\ \frac{1}{R_l+R_g}\{\frac{\overline{C_l}^2-\overline{C_l}}{2(\overline{C_l}-1)} + \frac{\overline{C_g}^2-\overline{C_g}}{2(\overline{C_g}-1)}\} & j = 3,6 \end{cases} \quad (2)$$

The term p_l is the probability that at least one local request is generated and no global request is generated while p_g be the probability that at least one global request is generated by a PE. Equations are given as below:

$$\begin{aligned} p_l &= [\,1 - (1-R_l)^N\,][1-R_g]^N \\ p_g &= [\,1 - (1-R_g)^N\,] \end{aligned}$$

The terms WIN_l and WIN_g are the probabilities that the local request (p_l) and global request (p_g) of a PE are selected by arbiter for memory access respectively. These are expressed as:

$$\begin{aligned} WIN_l &= \frac{p_l}{N\,R_l} \\ WIN_g &= \frac{p_g}{N\,R_g} \end{aligned}$$

The probability that a PE finds local bus busy at the beginning of the cycle, is denoted by the term $BUSY_l$ and $BUSY_g$ be the corresponding term for global bus. These are expressed as:

$$\begin{aligned} BUSY_l &= (N-1)(\overline{C_l}-1)\mu_1 + N(\overline{C_g}-1)\mu_4 \\ BUSY_g &= (N-1)(\overline{C_g}-1)\mu_4 + N(\overline{C_l}-1)\mu_1 \end{aligned}$$

State transition probabilities are deduced from the discussion of the model formulation given in Section III-B and represented in equation (3).

$$\alpha_j = \begin{cases} 1 & j = 0 \\ X_l(1-BUSY_l)^2\,WIN_l & j = 1 \\ X_l(1-BUSY_l)^2(1-WIN_l) & j = 2 \\ X_lBUSY_l(2-BUSY_l) & j = 3 \\ X_g(1-BUSY_l)WIN_l & \\ (1-BUSY_g)^2WIN_g & j = 4 \\ X_g(1-BUSY_g)[& \\ (1-BUSY_l)(1-WIN_l) & \\ +(1-BUSY_g)(1-WIN_g)] & j = 5 \\ X_g[BUSY_g + (1-BUSY_g) & \\ (BUSY_l + BUSY_g)] & j = 6 \end{cases} \quad (3)$$

$$\begin{aligned} \beta_j &= \alpha_j/X_k,\ X_k = X_l \text{ for } j = 1 \text{ and } X_k = X_g \text{ for } j = 4 \\ \overline{\beta_j} &= 1 - \beta_j \qquad \text{for} j = 1,4 \end{aligned}$$

Steady state probabilities are computed from (1)-(3) and are given in equation (4).

$$P_j = \begin{cases} \eta_0\,\beta_1\,R_l & j = 0 \\ \eta_1\,\beta_1\,R_l & j = 1 \\ \eta_2\,R_l\,(\alpha_2 + \alpha_3\overline{\beta_1}) & j = 2 \\ \eta_3\,R_l\,\alpha_3\,\beta_1 & j = 3 \\ \eta_4\,\beta_2\,R_g & j = 4 \\ \eta_5\,R_g\,(\alpha_5 + \alpha_6\overline{\beta}_2) & j = 5 \\ \eta_6\,R_g\,(\alpha_6\,\beta_2) & j = 6 \end{cases} \quad (4)$$

We use iterative algorithm to solve equations (1)-(3) to obtain steady state probabilities of the model. These probabilities are use to deduce performance parameters of HBB architecture as illustrated in the equation (5).

$$\begin{aligned} BW_l &= N\,P_1 \\ BW_g &= N\,P_4 \\ \overline{L_l} &= N\,(P_2 + P_3) \\ \overline{L_g} &= N\,(P_5 + P_6) \\ \overline{W_l} &= \eta_2(\alpha_2 + \alpha_3\overline{\beta_1})/\beta_1 + \eta_3\alpha_3 \\ \overline{W_g} &= \eta_5(\alpha_5 + \alpha_6\overline{\beta_4})/\beta_4 + \eta_6\alpha_6 \end{aligned} \quad (5)$$

IV. Results

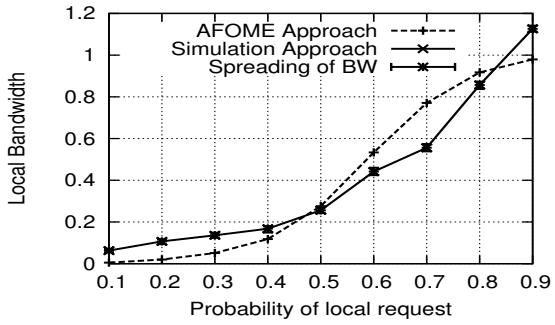

Fig. 3. Variation of local bandwidth with X_ℓ.

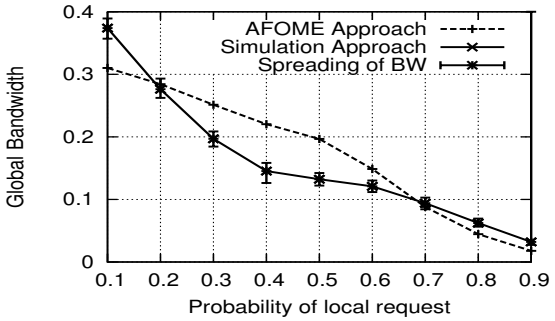

Fig. 4. Effect of X_ℓ on global bandwidth.

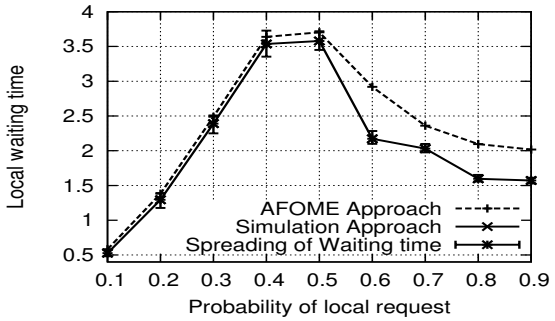

Fig. 5. Plot of local wait time with X_ℓ.

In this section, we present performance evaluation results of HBB architecture obtained using the proposed modeling approach. Results are compared with results of simulation of GSMP model. The simulation was performed on P-IV based linux-workstation with 1 GB RAM using *Stateflow* component of SIMULINK from Mathworks Inc.

Performance parameters of a PE mapped to the hierarchical bus were estimated with variation of probabilities of local request X_l and global request X_g. Input parameters are taken as $\overline{T} = 2$, $\overline{C_l} = 2$ cycles, $\overline{C_g} = 2$ cycles and $N = 2$. Result showing variation of BW_l with X_l = 0.1 to 0.9 (X_g = 0.9 to 0.1) is reported in Fig. 3 while Fig. 4 depicts effect of X_l on BW_g.

Figure 3 shows, BW_l increases with X_l, with small boost in the beginning because global requesting probability is higher than local requesting probability and global request has higher priority than local requests. Rate of increase is more beyond $X_l = 0.4$ with maximum local BW (0.9797) higher than maximum global BW (0.3101) as observed from figures 3 and 4. This is because two stage arbitration for BUS1 and BUS2 is essential for accessing global memory, so PE requesting for global memory has to wait in local as well as global waiting states and wins arbitration of both buses when both would become free. This infers that PE having higher communicating payload with memory should be mapped to the same bus as that of memory to achieve better performance similar to the explanation given in [8]. Thus designer could find optimum mapping early in design cycle. Figure 5 indicates that waiting

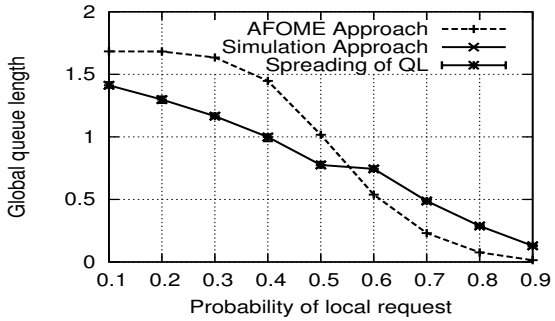

Fig. 6. Global queue length with X_ℓ

time for local request increases upto $X_l = 0.4$ as global request are dominating and then decline rapidly. Figure 6 depicts global queue length with X_ℓ.

V. Conclusions

This paper presents generalized semi Markov modeling technique for performance evaluation of HBB architectures. We have evaluated performance metric viz. local memory bandwidth (BW_ℓ), local average queue length at memory ($\overline{L_\ell}$) and local average waiting time seen by a PE ($\overline{W_\ell}$) for local memory MEM1; whereas in case of global memory, global memory bandwidth (BW_g), global average queue length at memory ($\overline{L_g}$) and global average waiting time seen by a PE ($\overline{W_g}$) for global memory MEM2. Proposed analytical approach took 0.0065 seconds while simulation taking 884.16 seconds and on an average 89 % accurate as compared with simulation.

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