Multi-objective Analog Circuit Sizing using SVM Macro-model as Evaluation function within Genetic Algorithm

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***Abstract*—Analog Circuit sizing is performed as part of synthesis in order to determine the sizes of all components in the circuit so that it is able to meet set of performance specifications. Stochastic combinatorial optimization methods such as simulated annealing and genetic algorithms are suited for faster determination of optimal sizes of the components. Set of multiple performance parameters for very large number of circuit sizing values are required by these algorithms. Therefore the reduction in time required to estimate these performance parameters is highly desired. For the purpose of estimation of performance parameters, we employ Support Vector Machine (SVM) based macro-models of analog circuits under consideration, instead of SPICE simulation. These SVM macro-models are not only faster to evaluate, but use of efficient kernel functions also make them almost as accurate as SPICE.**

In this paper, we have employed multi-objective genetic algorithm, which addresses the issue of simultaneously optimization of multiple performance parameters. We report the Pareto optimal points so obtained, satisfying more than one objective function. Least Square SVM toolbox interfaced with MATLAB was used for multi-variate SVM regression. HSPICE was used to generate data-set, which was used to train the SVM macro-model.

Keywords: Analog circuit sizing, macromodels, Support Vector Machine, kernel, regression, Pareto optimal points

I. Introduction

Circuit synthesis of analog circuit is to determine the size of all components in the circuit so that it is able to meet set of performance specifications [1], [2]. Optimum size of the components are determined using stochastic combinatorial optimization method such as simulated annealing and genetic algorithms. Performance parameters for great number of circuit sizing values is required by these algorithms. Therefore the reduction in time required to estimate these performance is of great benefit.

Performance functions are very nonlinear for large variation in the parameter space. Many macromodeling techniques have been proposed to match the performance to design parameters [3], [4], [5]. In this paper, we have used Support Vector Machine (SVM) [6], [7], [8] based macro-models to provide robust and accurate estimate of performance parameters for two stage op amp and cascode op amp. The utility of these models is demonstrated in circuit sizing method logy using multi-objective genetic algorithm optimization. The SVM models used in this chapter were trained using data generated directly from SPICE and therefore are able to provide SPICE level accuracy. Because the evaluation time for the SVM models is much less than that required by a full SPICE simulation, the models can be incorporated into a circuit synthesis algorithm used to optimize a fitness function based on performance parameter constraints.

SVM models can estimate function to great precision given a finite discrete set of training data. Hyper dimensional non linear functions are readily modeled using SVM. Once trained with particular functional mapping, the evaluation time of SVM model is fast. However, obtaining data from SPICE simulation and training the model is time consuming.

Performance Macromodeling usually consist of two steps: feasibility design space identification and performance macromodels generation. A feasibility design space is defined as a multidimensional space in which every design satisfies all the design constraints. The minimum set of constraints is the one that ensures the correct functionality of the given circuit topology. Performance macromodels are only constructed and thereby valid in the functionally correct design space. Support vector machines (SVMs) are used as classifier to identify the feasible design space of analog circuits and then as regressor to model performance function of the circuits.

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II. Background

A. SVM Classification

The classification is procedure to separate out infeasible design points from feasible ones [9]. A design point in design space is indicating a set of input design variables, while all such points together constitute input data to classifier. The technique of Support vector machines (SVMs) that has been successfully applied to solve many practical problems in various fields is used for generation of feasibility classifier models.

SVMs [6] were proposed originally in the context of machine learning, for classification problems on (typically large) sets of data which have an unknown dependence on (possibly many) variables. We consider each of N data points $x_k \in R^n, k = 1, ..., N$ to be associated with a label $y_k \in \{+1, -1\}$ which classifies the data into one of two sets. In the simplest SVM formulation, the problem of finding a general representation of the classifier $y(x)$ becomes that of the construction of a hyper-plane $\omega^T x_k + b$ which provides 'maximal separation $\frac{2}{\|\omega\|^2}$ between points x_k belonging to the two classes. This give rise to an optimization problem of the form

$$P : min_{\omega,b} \quad \frac{1}{2}\omega^T\omega \quad s.t. \quad y_k[\omega^T x_k + b] \geq 1, \tag{1}$$

where the $\frac{1}{2}\omega^T\omega$ term represents a cost function to be minimized in order to maximize separation. The constraints are formulated such that the nearest points x_k with labels [either +1 or -1] are (with appropriate input space scaling) at least $\frac{1}{\|\omega\|^2}$ distant from the separating hyper-plane. To solve this 'primal minimization problem, we construct the dual maximization of eqn. (1) using the Lagrangian form

$$D : \max_{\alpha} \mathcal{L}(w, b; \alpha), \tag{2}$$

where

$$\mathcal{L}(\omega, b; \alpha) = \frac{1}{2}\omega^T\omega - \sum_{k=1}^{N} \alpha_k(y_k[\omega^T x_k + b] - 1), \tag{3}$$

and α_k are the Lagrange multipliers. After applying the conditions for optimality

$$\frac{\partial\mathcal{L}}{\partial\omega} = 0, \frac{\partial\mathcal{L}}{\partial b} = 0, \frac{\partial\mathcal{L}}{\partial\alpha_k} = 0, \tag{4}$$

and eliminating ω by expressing it in terms of $\alpha = [\alpha_1, ..., \alpha_N]$, we arrive at a Quadratic Programming (QP) problem

$$min(\alpha Q\alpha + B\alpha), \tag{5}$$

for suitably defined matrices Q, B. Having solved for α, the following classifier representation is obtained

$$y(x) = sign\left[\sum_{k=1}^{\#SV} \alpha_k y_k x_k^T x + b\right]. \tag{6}$$

Here #SV represents the number of non-zero Lagrange multipliers α_k, called support vectors, corresponding to input data x_k. The SVM representation will be sparse if only a few of the input data, called support vectors, are 'near to the separating hyper-plane. A key feature of the Support Vector Machines is the ability to replace the input data by a non-linear function $\phi(x)$ operating on the input data. This may be viewed as mapping the input data to higher dimensional space, to enable classification of data that is not linearly separable in the original input space. To do this, we formally replace $x_k^T x$ (the dot product between a support vector x_k and any point x of the input space) in eqn. (11) by $\phi(x_k)^T\phi(x)$ to represent the action of this mapping, obtaining

$$y(x) = sign\left[\sum_{k=1}^{\#SV} \alpha_k y_k \phi(x_k)^T\phi(x) + b\right]. \tag{7}$$

In the cases where $\phi(.)$ is infinite-dimensional, we invoke the so-called 'kernel trick': the expression $\phi(x_k)^T\phi(x)$ may under certain conditions be replaced by a Kernel function $K(x_k, x)$. An equivalent interpretation is that the kernel function is a suitably-defined dot product $< x_k, x >$ replacing $x_k^T x$ in the Hilbert space defined by the mapping ϕ. In this way, we avoid ever having to represent the mapping ϕ explicitly. In either case, the use of a kernel function allows the SVM representation to be independent of the dimensionality of the input space. There are different kernel functions that provide the SVM, the ability to model complicated separation hyperplanes. We use the efficent kernel proposed in [10] to buit SVM model for classifying feasible design space.

Widths of the transistors, coupling capacitor and bias currents are chosen as design variables. In order to generate input data set, values of these design variables for a given circuit are randomly generated within upper and lower bounds of geometrical constraints. A known instance of all the design variable is considered a tuple. HSPICE is used on each of these tuples of design variables to evaluate performance and verify functional and performance constraints. For given set of tuples which satisfy both functional and performance constraints, output is taken as '1' otherwise as '-1' . This forms set of input and output data pair. Some of these data pairs are used to train SVM classifier and while the remaining are used for validation i.e. to check the accuracy of classifier.

B. SVM Regression

In the case of function regression, the labels $y_k \in \{-1, +1\}$ represented by the $\{+1, -1\}$ valued function $y(x)$are replaced by the real valued $y_k \in R$. Further by a certain nonlinear mapping ϕ, the training pattern x_t is mapped into some feature space, in which a real valued function $y(x)$ is defined as follows.

$$y(x) = \omega^T\phi(x) + b \text{ with } \omega \in R^N, b \in R \tag{8}$$

$\phi(.) : R^n \rightarrow R^{n_h}$is the mapping to the high dimensional and potentially infinite dimensional feature space.

For the Least-Squares SVM regression error variables for the fitting problem are:

$$e_k = w^T\phi(x_k) + b - y_k \; k = 1, ..., N \tag{9}$$

Given a training set $\{x_k, y_k\}_{k=1}^N$ following optimization problem is formulated in the primal weight space.

$$P : \min_{w,b,e} J_p(w, e) \quad = \quad \frac{1}{2}w^T w + \gamma\frac{1}{2}\sum_{k=1}^{N} e_k^2 \tag{10}$$

together with the N constraints [9]. This formulation involves the trade off between a cost function term and a sum of squared errors governed by the trade-off parameter γ. In the regression formalism the term $\frac{1}{2}w^T w$ is no longer related to hyper-plane separation, but instead determines the smoothness of the resulting model. In fact, the primal problem in the LS-SVM formalism is wholly equivalent to a ridge regression problem formulated in the feature space, with parameter γ performing the role of smoothing parameter. Proceeding to the dual Lagrangian-based formulation

$$D : \max_{\alpha} \mathcal{L}(w, b, e; \alpha) \tag{11}$$

$$\mathcal{L} = J_p(w, e) - \sum_{k=1}^{N} \alpha_k\{w^T\phi(x_k) + b + e_k - y_k\} \tag{12}$$

where α_k are Lagrange multipliers. The conditions for optimality are given by

$$\begin{cases} \frac{\partial\mathcal{L}}{\partial w} = 0 \; \rightarrow \; w = \sum_{k=1}^{N} \alpha_k\phi(x_k) \\ \frac{\partial\mathcal{L}}{\partial b} = 0 \; \rightarrow \; \sum_{k=1}^{N} \alpha_k = 0 \\ \frac{\partial\mathcal{L}}{\partial e_k} = 0 \; \rightarrow \; \alpha_k = \gamma e_k, \qquad k = 1, ..., N \\ \frac{\partial\mathcal{L}}{\partial \alpha_k} = 0 \; \rightarrow \; w^T\phi(x_k) + b + e_k, - y_k = 0, \qquad k = 1, ..., N \end{cases} \tag{13}$$

After elimination of the variables w and e one gets the following solution

$$\begin{bmatrix} 0 & 1_N^T \\ 1_N & \Omega + I/\gamma \end{bmatrix} \begin{bmatrix} b \\ \alpha \end{bmatrix} \quad = \quad \begin{bmatrix} 0 \\ y \end{bmatrix} \tag{14}$$

where $[y_1; ...; y_N]$, $1_v = [1; ...; 1]$and $\alpha = [\alpha_1; ...; \alpha_N]$.
The kernel trick is applied here as follows

$$\begin{aligned} \Omega_{kl} \quad &= \quad \phi(x_k)^T\phi(x_l) \\ &= \quad K(x_k, x_l) \qquad k, l = 1, ..., N \end{aligned} \tag{15}$$

The resulting LS-SVM model for function estimation becomes then

$$y(x) = \sum_{k=1}^{N} \alpha_k K(x, x_k) + b \tag{16}$$

where α_k, b are the solution to the linear system [14] .

The function $k(x, x_k)$corresponds to a dot product in some feature space.

SVM models are typically trained with a discrete set of data points called the training data set. This represent performance functionality of circuit being modeled. It is not necessary to know the internal structure of a system in order to model it using SVM model, it is necessary to have examples corresponding to the behavior between the inputs and outputs. This set of example data is the training data set. A second set of discrete data points not present in the training data set is used to validate the SVM model of the system.

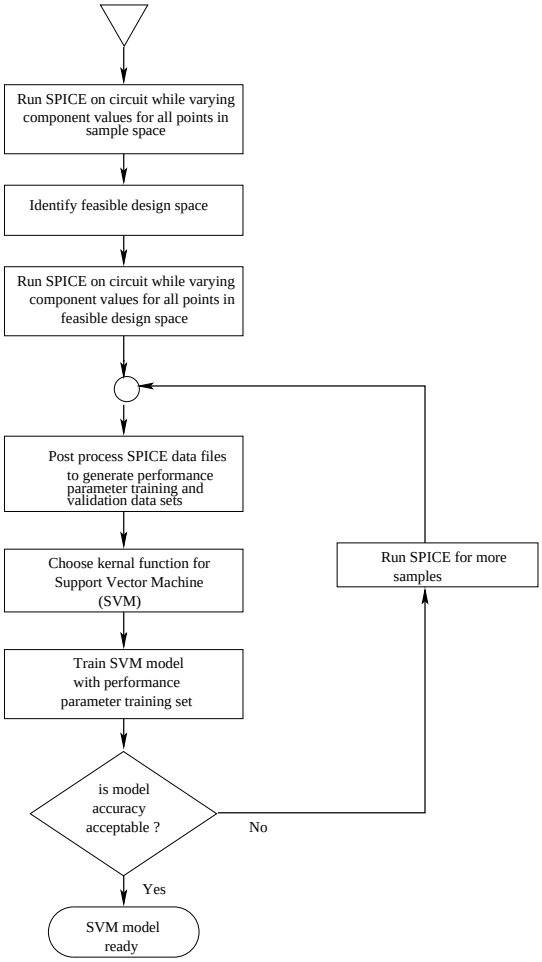

Figure 1. Flow diagram of SVM model development.

The circuit simulator HSPICE is used to calculate several standard performance parameters describing the functionality of operational amplifier circuit. By doing SPICE simulation for many combinations of op amp transistor sizes, training and validation data sets are produced. These are then used to generate SVM model for the performance parameter. A general iterative methodology as suggested in [10] is used for SVM model development and is reproduced in Figure 1. The correlation coefficient of various performance parameters of two stage op-amp is shown in Figures 4, 5 and 6. The correlation coefficients are found close to one, which implies that models are quite accurate.

After training, the SVM model for given op amp topology is used to provide estimates of op amp performance parameter during optimization. Op amp under various performance constraints is then synthesized using a genetic algorithm. The output of the genetic algorithm is a sized op amp circuit meeting constraint specification. Performance parameters of sized circuit are then verified through HSPICE. The block diagram in Figure 2 depicts the synthesis methodology using the SVM models.

III. Experimental setup

A. Two Stage op-amp

A single output two-stage op-amp is shown in Figure 3 . The circuit has 8 transistors, compensation and load capacitance and a reference bias current. The length of all transistors are fixed to a 1μm . This immediately eliminates nearly half of the free design parameters.

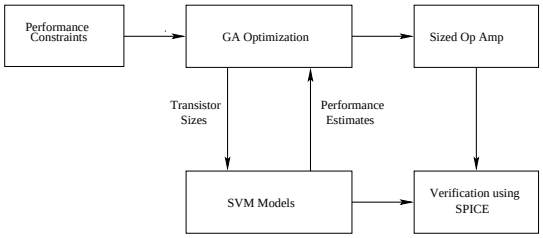

Figure 2. Block diagram of circuit synthesis via a genetic algorithm optimization engine with SVM models providing performance parameter estimates.

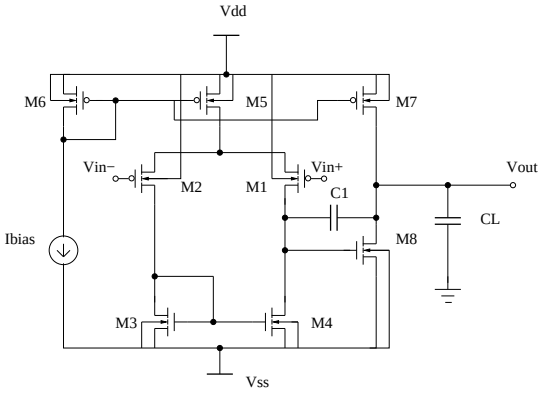

Figure 3. Two stage op amp

Further the size of transistor M1 should equal M2, and the size of M3 should equal M4 to equalize the currents through the differential pair. Both $W_1 = W_2$ and $W_3 = W_4$ are left as free parameters. Transistor M6 can be fixed to some minimum nominal size since its job is to simply mirror the reference current Ibias, which can also be fixed. The width of transistors M5 and M7 control the current through the differential pair and output stage respectively and are also left as free parameters.In order to minimize the DC offset voltage at the output node, width of transistor M8 is taken as $2 * W_3 * W_7 / W_5$. Lastly the compensation capacitor is left as a free variable since it controls the inherent stability of the op-amp. The load capacitor is taken as fixed variable to simplifying the modeling problem. The above arguments result in the 5-dimensional parametric configuration for the two-stage op-amp. The design variables and geometry constraints are shown in Table I. Functional and Performance constraints are shown in Table II. The functional constraints ensure all the transistors are on and in saturation region with some margin. We set $V_{on,min}$ and $V_{sat,min}$ to 0.1V.

Table I
Design Variables of Two stage Op amp

Design parameters	Geometric constraints
$W_1 = W_2$	[1μm,100μm]
$W_3 = W_4$	[1μm,50μm]
W_5	[1μm,100μm]
W_7	[1μm,100μm]
Cc	[5pF,20pF

Table II
Design constraints of Two-stage op-amp

Functional constraints	$V_{gs} - V_{th} \geq V_{on,min}$
	$V_{ds} \geq V_{gs} - V_{th} + V_{sat,min}$
Performance constraints	Phase Margin $\geq 45^o$

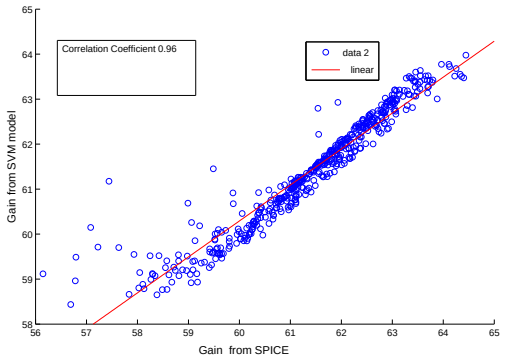

Figure 4.

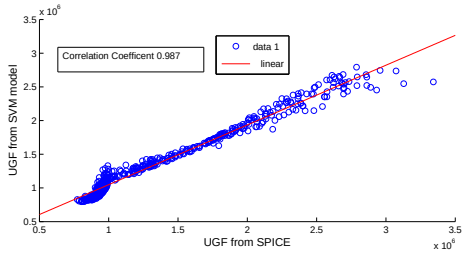

Figure 5.

B. Cascode Op amp

The circuit of cascode op-amp is shown in Figure 7. We fix the lengths of all transistors to 1μm. Imposing sizing rules [11] similar to that of two-stage op-amp we get five design variables for cascode op-amp. Load capacitance is set to 1pf. The design variables and geometry constraints are shown in Table III. Other constraints shown in Table IV. The functional constraints ensure all the transistors are on and in saturation region with some margin. We set $V_{on,min}$ and $V_{sat,min}$ to 0.1V.

Least Square SVM toolbox interfaced with MATLAB was used for developing the classifier to identify feasible design space. Data in feasible design space was used to develop SVM regressor models for different performance parameters of two stage op amp and cascode op amp like phase margin, unity gain frequency, CMRR, PSRR and slew rate.

C. Sizing

Op amp under various performance constraints is then synthesized using genetic algorithm. Genetic algorithm is chosen since it is robust in the presence of multiple constraints and is insensitive to the nature of the cost function. Genetic algorithm have been successfully used previously for synthesis of analog circuits [12], [2]. The block

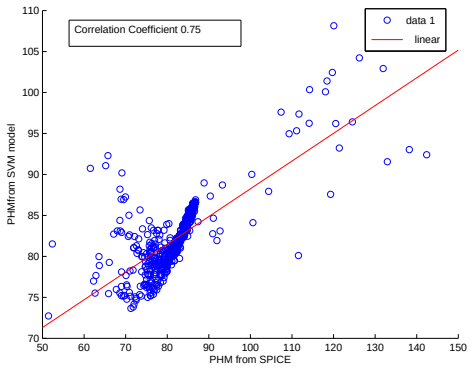

Figure 6.

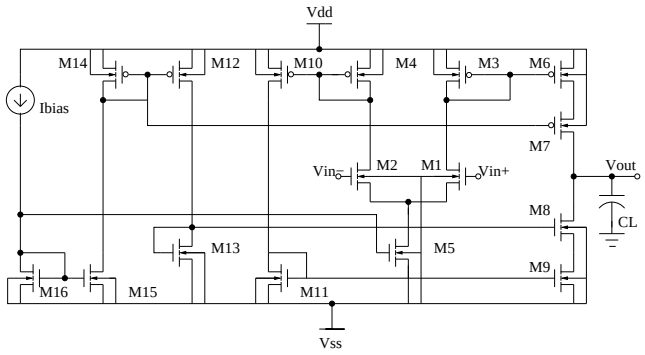

Figure 7. Cascode Op amp

Table III
DESIGN VARIABLES OF CASCODE OP-AMP

Design parameters	Geometric constraints
$W_1 = W_2$	[1μm,100μm]
$W_3 = W_4$	[1μm,100μm]
$W_5 = W_6$	[1μm,100μm]
Ibias	[2μA,20μA]
C_L	[1pF,10pF]

diagram in Figure 2 depicts the synthesis methodology using the SVM models. The output of genetic algorithm is a sized op amp circuit meeting constraint specifications. GA toolbox of MATLAB was used to run genetic algorithm to size the two stage op amp and cascode op amp with objective function to minimize area and at same time satisfying performance constraints given in Table V and Table VI. It was run for 100 generations with population size of 20. Crossover function used was scattered and the mutation function selected was Gaussian. Elite count was taken as 2 and crossover fraction 0.8.

IV. RESULTS

The dimensions of transistors, compensation capacitor and bias current of two stage op amp and cascode op amp optimized for minimum area and constraints, obtained through genetic optimization algorithm are shown in Table VII and Table IX respectively. Values of performance parameter obtained through HSPICE as well as SVM models is also shown in Table VIII and Table X respectively. All the performance parameter satisfy the constraint specified in sizing algorithm.

V. PARETO OPTIMAL SURFACE

Often, a number of parameters in the performance functions compete against each other. Hence, selecting the design variable

Table IV
DESIGN CONSTRAINTS OF CASCODE OP-AMP

Functional	$V_{gs} - V_{th} \geq V_{on,min}$
constraints	$V_{ds} \geq V_{gs} - V_{th} + V_{sat,min}$
Performance constraints	Phase Margin $\geq 60^o$

Table V
PERFORMANCE CONSTRAINTS FOR TWO STAGE OP AMP

Performance	Constraints
Open-loop gain	$\geq 60\,dB$
Phase-margin	$\geq 70^\circ$
Unity-gain frequency (UGF)	$\geq 2\,MHz$

Table VI
PERFORMANCE CONSTRAINTS FOR CASCODE OP AMP

Performance	Constraints
CMRR	$\geq 100\,dB$
PSRR	$\geq 120\,dB$
Phase-margin	$\geq 70^{\circ}$
Slew rate	$\geq 1.25e06$
Unity-gain frequency (UGF)	$\geq 1e06$

Table VII
VALUES OF DESIGN VARIABLES FOR OPTIMIZED TWO STAGE OP AMP

Design Variable	Optimal Size
$W_1 = W_2$	$6.482e-05$
$W_3 = W_4$	$9.631e-06$
W_5	$2.870e-05$
W_7	$6.500e-05$
Cc	$6.796e-12$

such that one of the performance parameter is optimal will generally not result in optimal values for other parameters. Thus, the circuit optimization problem turns out to be a multi objective optimization problem. For competing objective functions, it is not feasible to maximize the performance of all of them. Then one has to make trade-offs between different performance parameters. Enhancing of one performance parameter may result in diminishing of other.

Let there be vector of objectives

$F(x) = [F_1(x), F_2(x), ..., F_m(x)]$

that must be traded off.

Multi-objective optimization is concerned with the minimization of a vector of objectives $F(x)$ that can be the subject of a number of constraints or bounds.

$$\min_{x \in R^n} F(x) \;\; subject\ to \;\; G_i(x) = 0,\ i = 1, ..., k_e;\ G_i(x) \leq 0,\ i = k_{e+1}, ..., k;\ \ and \;\; l \leq x \leq u$$

As $F(x)$ is a vector and components of F_x are competing there is no unique solution to this problem. Concept of Pareto optimality is used to characterize such competing objectives. A Pareto optimal solution is one in which an improvement in one objective requires a degradation of another.

Let us consider a feasible region, Ω, in the parameter space. X is an element of the n-dimensional real numbers $x \in R^n$ that satisfies all the constraints i.e.,

$\Omega = \{x \in R^n\}$, subject to

Table VIII
VALUES OF PERFORMANCE PARAMETER FOR OPTIMIZED TWO STAGE OP AMP

Performance Parameter	(HSPICE)	(SVM-Model)
Open-loop gain	$61.71\,dB$	$61.23\,dB$
Phase-margin	122°	133°
UGF	$2.75\,MHz$	$3.05\,MHz$

Table IX
VALUES OF DESIGN VARIABLES FOR OPTIMIZED CASCODE OP AMP

Design Variable	Optimal Size
$W_1 = W_2$	$2.600e-05$
$W_3 = W_4$	$9.846e-06$
$W_5 = W_6$	$7.871e-05$
Ibias	$1.727e-05$
C_L	$3.702e-12$

Table X
VALUES OF PERFORMANCE PARAMETER FOR OPTIMIZED CASCODE OP AMP

Performance Parameter	(HSPICE)	(SVM-Model)
CMRR	$143\,dB$	$139\,dB$
Phase-margin	71°	70°
PSRR	$151\,dB$	$136\,dB$
Slew rate	$1.76e06$	$1.43e06$
UGF	$1.48e06$	$1.29e06$

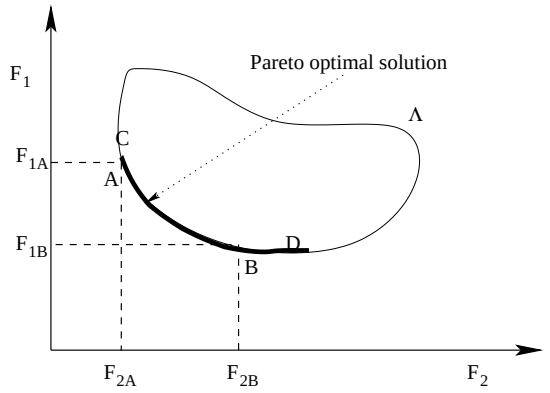

Figure 8. Set of Pareto optimal solution

$G_i(x) = 0, i = 1, ..., k_e,$

$G_i(x) \leq 0, i = k_{e+1}, ..., k,$

$l \leq x \leq u.$

Definition of the corresponding feasible region for the objective function space Λ

$\Lambda = \{y \in R^m : y = F(x), x \in \Omega\}$.

The performance vector F(x) maps parameter space into objective function.

A. Pareto optimal solution

Point $x^* \in \Omega$ is a Pareto optimal solution if for some neighborhood of x^*there doest not exist a Δx such that $(x^* + \Delta x) \in \Omega$ and

$F_i(x^* + \Delta x) \leq F_i(x^*),\ i = 1, ..., m,$ and

$F_j(x^* + \Delta x) \leq F_j(x^*)$ for at least one j.

In the two dimensional representation of the Figure 8 , the set of Pareto optimal solution lies on the curve between C and D. Points A and B represent specific Pareto optimal points because an improvement in one objective, F_1, requires a degradation in the other objective, F_2, i.e., $F_{1B} < F_{1A}$, $F_{2B} > F_{2A}$

The Pareto curve is the set of $x^*$where there are no other solutions for which simultaneous improvement in all objectives can occur.

A general goal in multi-objective optimization is constructing the Pareto optima. We use GA-multi-objective tool box in MATLAB to create a set of Pareto optima. It uses genetic algorithms to identify Pareto points.

B. Multi-objective Sizing of op amp

Using multi-objective genetic optimization [13], the surface of Pareto-optimal design point is calculated for three performance parameters of two stage op amp. Performance parameters that are considered are open-loop gain, phase-margin and unity gain frequency. Multivariate regression model is developed using SVM of two stage op amp for the above three output performance function of op amp. The multivariate model has SPICE level accuracy as it is trained by data obtained through SPICE simulation and is quite fast in evaluation

Table XI
PARETO-OPTIMAL DESIGN VARIABLES OF TWO STAGE OP AMP

$W_1 = W_2$ (in μm)	$W_3 = W_4$ (in μm)	W_5 (in μm)	W_7 (in μm)	Cc (in pf)
70.59	7.51	38.80	74.91	11.81
73.23	4.49	47.53	65.84	13.41
68.96	11.13	61.09	26.83	12.98
47.56	12.16	60.16	25.49	10.19
73.17	4.49	48.09	65.74	13.07
73.02	8.81	40.79	71.69	11.83
70.04	10.86	40.42	53.73	12.12
71.09	8.59	39.78	51.18	12.01
71.58	10.97	47.17	46.46	12.20
74.96	12.22	41.28	65.81	12.18
71.26	16.38	43.03	50.24	13.16
71.96	5.65	47.38	70.22	12.51
72.17	8.27	48.22	39.69	12.38
69.87	10.90	60.02	52.88	12.76

Table XII
PARETO-OPTIMAL PERFORMANCE PARAMETER OF TWO STAGE OP AMP

Open-loop gain (in dB)	Phase-margin (in degrees)	Unity-gain frequency (in MHz)
61.17	155	3.02
60.07	106	3.15
64.76	85	0.89
63.81	86	0.86
59.98	107	3.13
61.52	140	3.03
62.65	88	2.21
62.44	93	2.17
63.28	72	1.79
62.16	99	2.84
63.07	71	1.98
60.57	113	3.06
63.70	81	1.37
62.66	67	2.07

of circuit performances for given set of design variables. This models is then used within multi-objective genetic algorithm to generate set of Pareto-optimal points. These Pareto-optimal points help designer to know trade-off between different performance function of circuit. For every point on the performance space boundaries, the required set of design variables can be retrieved and hence helpful in sizing the circuit. The Pareto-optimal design variables as well as performance parameters obtained for two stage op amp using GA-multi-objective is shown in Table XI and Table XII respectively. It was run for 122 generations with population size of 60. Crossover function used was scattered with crossover fraction of 0.8.

VI. CONCLUSIONS

We have proposed multi-objective GA based on SVM macromodels for analog circuit sizing. The analog macro-models replace Spice simulators, used for circuit fitness evaluation inside GA, consuming very little time and are almost as accurate as Spice. We formulate the SVM macro-model using multi-variate regression using efficient kernel function for SVM. Multi-objective nature of optimal sizing provides much desired Pareto points in design space corresponding to appropriate sizes of devices. Our further work includes the tuning of kernel parameters as well as GA parameters, which enhance the optimality of solution.

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