Interactive Generalized Semi Markov Process Model for Evaluating Arbitration Schemes of SoC Bus Architectures

Ulhas Deshmukh, Research Scholar,
Deptt. of Electronics & Comm. Engg.
MNIT Jaipur, India
deshmukhur@gmail.com

Vineet Sahula, *SMIEEE*, Associate Professor,
Deptt. of Electronics & Comm. Engg.
MNIT Jaipur, India
sahula@ieee.org

Abstract

Ever increasing component counts of a System-on-Chip makes communication among components complex and diverse. Thus communication architecture becomes a major performance determining candidate. This paper proposes a formal technique for system level performance analysis that can help the designer to select the appropriate arbitration scheme for a chosen bus-based communication architecture. For a bus with arbitration, we formulate a model based on interacting generalized semi Markov process. We mainly focus on building model for single shared bus architecture and explore arbitration along with different priority schemes viz. (i) fixed, (ii) lottery based and (iii) round robin. We describe the model of bus architecture using these arbitration schemes in the Stateflow component of MATLAB. Our modeling approach provides an evaluation and comparison of performance parameters viz. memory bandwidth, processing element utilization, average queue length at the memory and average waiting time seen by a processing element, for a chosen arbitration scheme.

1. Introduction

Performance of electronic systems in diverse and emerging application areas like telecommunication and multimedia significantly improves by using System-on-Chip (SoC) paradigm. System-on-Chip design methodology involves two issues- (i) allocation and mapping of system computation to the set of high performance computing elements, and (ii) selection of appropriate communication architecture that provides communication between these computing elements. These computing elements, which are often called Intellectual Property (IP) blocks, are predesigned and pre-verified in the form of hardware or software. Hardware IPs generally include embedded processor (DSP,CPU), memory blocks, Application Specific Integrated Circuits (ASICs), analog blocks and interface blocks. Software IPs usually include Real Time Operating System (RTOS) and device drivers. In order to satisfy demand for higher performance and complex functionality, designer tend to use heterogeneous IPs. Therefore, communication requirement becomes not only diverse but also complex and hard to satisfy. In this scenario, communication architecture emerges as a major performance determining component of SoC design. In this paper, we are concerned about bus-based communication architectures since they are still the most widely used in low end high volume SoC and embedded applications, due to their simplicity and popularity.

However, even after selection of architecture trade off between parameters such as, number of buses, topologies, mapping of Processing Elements (PEs) and arbitration policy is crucial. Each of these factors has remarkable impact on system performance.

In this paper, we propose a formal technique for system level performance analysis of a Single Shared Bus (SSB) communication architecture. In particular, we explore arbitration schemes with various priority schemes viz. fixed, lottery based and round robin. In Section 2, we present an overview of performance estimation techniques, while in Section 3 an analytical formulation based on Generalized Semi Markov Process (GSMP) for performance evaluation for single shared bus is given. When PEs are heterogeneous, we propose an extension to model based on Interacting GSMP (IGSMP) framework in Section 4. In Section 5, we present the results. We conclude in Section 6.

2. Performance estimation of communication architecture: an overview

Communication architecture allows exchange of data and control signals between various system components. Communication architectures can be broadly classified as bus-based, Network-on-Chip (NoC) based [6] or Hybrid bus-NoC based architectures [11]. Bus based architectures

978-0-7695-3325-4/08 $25.00 © 2008 IEEE
DOI 10.1109/EMS.2008.77

have different variants including single shared bus, network of shared buses or even dedicated buses. In SoCs and embedded applications, designers have been using bus based architectures since long because these are simple, consume less power and form the primitive architecture in complex communication. Moreover, bus based architectures not only meet demands of communication but also result for cheaper design in low end and high volume applications.

Various arbitration schemes are employed in shared bus architectures to resolve the bus access conflict. (i) Fixed or static priority based arbitration is a common arbitration policy used in the shared bus architectures. With fixed priority arbitration, each master is assigned a unique priority level. When more than one master request for the bus, arbiter resolve the conflict and the highest priority master wins the arbitration and gains control of the bus. (ii) In lottery based arbitration scheme, priorities to the masters are assigned randomly. (iii) Round robin arbitration can be classified as being Fixed Slot Allocation (FSA) arbitration and Idle Recovery Slot Allocation (IRSA) arbitration. In FSA arbitration, the slot time for a master is reserved, regardless of whether the master uses the time slot. In contrast, the IRSA round robin allows time allocated for a given master which is no longer required to be used by other master.

2.1. Related work

Many approaches for performance evaluation of on chip communication architectures have been proposed in literature- Simulation based approach uses communication models at various levels of abstraction. Work in [9] presents simulation by abstracting the system at cycle count accurate at transaction boundaries. Authors in [13] propose formal concurrent modeling approach based on Operation State Machine (OSM) for entire system comprising of computation and communication. Authors in [3] introduce worst case static performance analysis of the system comprising concurrent communicating processes. Work in [2] proposes formal modeling approach based on GSMP model and evaluation based on Analytical Formulation of Model Equations (AFOME) to estimate performance metrics of a SSB architecture. Two phase hybrid approach encompasses simulation based and analytical approaches to exploit benefits of both [4] [5]. In [5] authors perform initial co-simulation with the abstracted communication and then analytical analyzed by specifying communication architecture. Queueing analysis in [4] uses analytical approach to prune the design space and then entire system simulation of the selected architectures. Application of interacting Markov chains for modeling cellular signal processing in biological cell have been presented in [7]. Authors in [1] propose influence model comprising network of interacting Markov chains. Stochastic Automata Network (SAN) model described in [8] is quite similar to interacting Markov chains.

2.2. Contribution of the paper

Chief contribution of the paper lies in the proposal for system level framework based on IGSMP model for performance estimation of communication architecture. We mainly focus on building model for SSB architecture and explore arbitration with different priority schemes viz. fixed, lottery based and round robin. We present high level simulation model of each of the aforementioned arbitration schemes based on IGSMP model in the Stateflow component of MATLAB. Our modeling approach provides estimation of performance parameters viz. memory BandWidth (BW), Processing element Utilization (PU), average queue length ($\overline{L}$) at memory and average waiting time ($\overline{W}$) seen by a PE. The input parameters to the model are number of PEs (N), the mean computation time ($\overline{T}$) and first and second moment of connection time of PEs ($\overline{C}$, $\overline{C^2}$).

3. GSMP model for single shared bus architecture: An overview

In this section, we review GSMP model of a PE mapped to SSB architecture, assuming that all PEs are homogeneous. We present Analytical Formulation of the Model Equations (AFOME) approach [2] for evaluation of performance metrics.

The SSB architecture consisting of N PEs, PE_1, PE_2,...,PE_N competing for the use of a bus (BUS), for accessing shared memory (MEM) is depicted in Fig. 1. Communication between PEs and shared memory of the system is assumed to be synchronous with system bus cycle. Arbiter of N-user one-server type is employed to resolve the bus access conflict among PEs. All PEs are assumed to be identical and hence GSMP model of a PE suffices for functional modeling [12]. Let us consider a scenario when a PE mapped to the BUS attempts to access MEM. Figure 2 shows GSMP model of a PE in this scenario, which has four states. In computing state (*state 0*) a PE performs computation. Accessing state labelled as *state 1*, corresponds to the situation when a PE is accessing MEM. In full waiting state labelled as *state 2*, a PE waits for MEM for full connection time of another PE accessing MEM; while in residual waiting state labelled as *state 3*, a PE waits for MEM for residual connection time of that another PE accessing MEM. In each state, model spends random amount of time with mean value η_i, called mean sojourn time of i^{th} state ($i = 0, 1, 2, 3$).

The input parameters to the model are number of PEs (N), the mean think time of PE ($\overline{T}$) and the first and second moment of connection time between PE and memory ($\overline{C}$, $\overline{C^2}$). For computation of transition probabilities, we

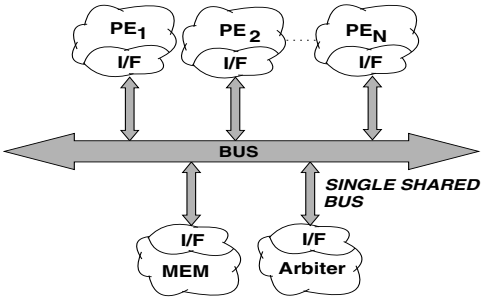

Figure 1. Single shared bus communication architecture.

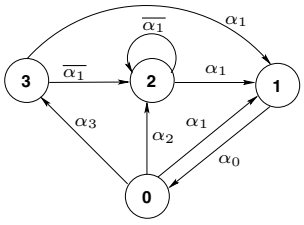

Figure 2. GSMP model of a PE in the single shared bus architecture.

define following parameters: (1) The probability of leaving i^{th} state is μ_i. (2) $R = \mu_0 + \mu_2 + \mu_3$, is the probability that a PE generates a request. (3) Probability of at least one request is, $p = [1 - (1 - R)^N]$. (4) Sojourn time of the states are, $\eta_0 = \overline{T}$, $\eta_1 = \eta_2 = \overline{C}$ and $\eta_3 = (\overline{C^2} - \overline{C})/(2(\overline{C} - 1)$. (5) The probability of wining arbitration is $WIN = p/NR$. (6) The term, $BUSY = (N-1)(\overline{C}-1)\mu_1$ is the probability that a PE finds bus or memory busy.

Transition from *state 0* to *state 1* takes place, when MEM and BUS both are idle with the probability $(1 - BUSY)^2$ and request wins arbitration with the probability WIN. Alternatively, GSMP transits from *state 0* to *state 2* when MEM and BUS are idle and local request does not win arbitration with the probability $(1 - WIN)$. Similarly, GSMP makes transition from *state 0* to *state 3* if at the time of request either (i) MEM is busy or (ii) MEM is idle but BUS is being used by PEs mapped to other bus. Pending requests of *state 2* and *state 3* are reconsidered after elapse their mean sojourn times and (a) if granted access, a PE enters to *state 1*, (b) otherwise it enters in the *state 2*. From *state 1*, the process always returns to *state 0*. State transition probabilities are deduced from discussion of the model as follows:

$$\alpha_j = \begin{cases} 1 & j = 0 \\ (1 - BUSY)^2\, WIN & j = 1 \\ (1 - BUSY)^2(1 - WIN) & j = 2 \\ BUSY(2 - BUSY) & j = 3 \end{cases}$$

We iteratively solve model equations to compute steady state probabilities of the model viz. $P_0 = \eta_0\alpha_1 R$, $P_1 = \eta_1\alpha_1 R$, $P_2 = \eta_2\, R(\alpha_2 + \alpha_3\overline{\alpha}_1)$, $P_3 = \eta_3 R\alpha_3\alpha_1$, where $\overline{\alpha_1} = (1 - \alpha_1)$. These probabilities are use to deduce performance parameters of a SSB architecture as illustrated in the equation (1).

$$\begin{array}{rcll} BW & = & NP_1 & \overline{W} = (\eta_2\alpha_2 + \eta_3\alpha_3)/\alpha_1 \\ PU & = & P_0 + P_1 & \overline{L} = N(P_2 + P_3) \end{array} \quad (1)$$

4. Model formulation for heterogeneous SSB architecture

The concept of interaction in various forms has been widely discussed in the literature. Depending on applications, interaction models have different structures such as, influence model [1] and interacting model [7].

In this section, we apply the modeling concept of interacting model and propose IGSMP model, for evaluating performance of the SSB architecture with heterogeneous PEs. We use bottom up approach to formulate IGSMP model from the underline interacting embedded Markov model [7]. Functional characteristic of an abstract system is shown in Fig. 1, which can be described in terms of its constituent components, that are PEs refereed as modules or nodes. These modules are heterogeneous and behave concurrently to execute system functionality, while communication between them and memory is sequential.

4.1. IGSMP model

IGSMP model, we employ consists of a network of N interacting GSMPs, X_1, X_2,..., X_N corresponding to the dynamics of PE_1, PE_2,...,PE_N respectively. Fig 3 shows IGSMP model for SSB architecture. Each GSMP model has four states, as discussed in Section 3. GSMP model at each module is composed of underlying embedded Markov model with Markovian property, that is the state $X_p[n]$ of the module X_p at time n is given by: $P(X_p[n] = j|X_p[n - 1] = i, ..., X_p[0] = m) = P(X_p[n] = j|X_p[n - 1] = i) = p_{ij}^{X_p}[n]$. In the absence of interaction, each module behaves independently and transition probability of embedded Markov model X_p is written as: $p_{ij}^{X_p}[n] = q_{ij}^{X_p}[n]$. Where, $q_{ij}^{X_p}[n]$ is independent of all the states of other modules in the network. So, limiting probability P_i of being in state i of the IGSMP model, which has independent GSMP models is

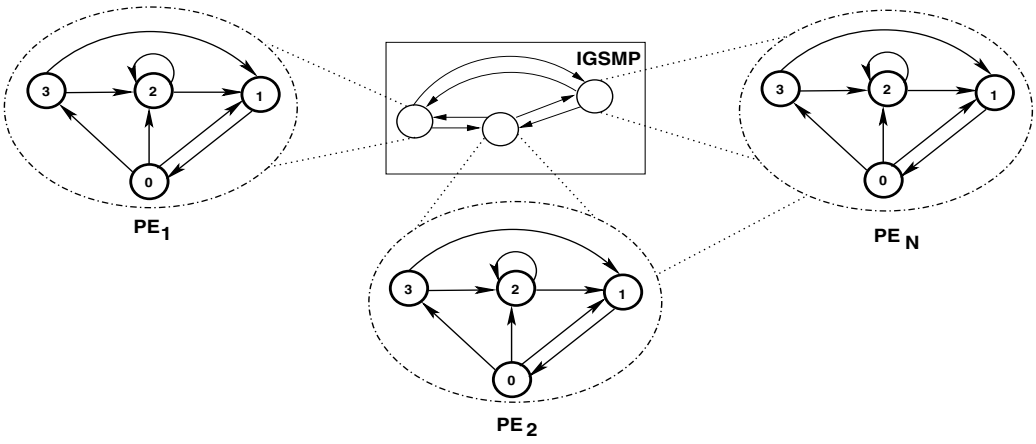

Figure 3. Interactive GSMP model for SSB communication system of heterogeneous PEs.

given in terms of limiting probabilities, π_i of the underline model and sojourn times, η_i as:

$$P_i = \frac{\pi_i \, \eta_i}{\sum_{j=0}^{N} \pi_j \, \eta_j}$$

As MEM and BUS are shared, behavior of PEs have influences on each other, the interaction between different modules are defined by influences of states in one module onto the transition probabilities in another module. Two types of influences are possible either positive or negative. In the proposed IGSMP model, only negative influences are present. In particular, if state ℓ of module X_r influences the transition probability $p_{ij}^{X_p}$ from state i to the state j in the module X_p, then $p_{ij}^{X_p}$ at time n due to influence of state ℓ in X_r, $\{p_{ij}^{X_p}[n]\}_{[\ell,X_r]}$ is written as follows.

$$\{p_{ij}^{X_p}[n]\}_{[\ell,X_r]} = \alpha_{r,\ell} f\{P(X_r[n-1] = \ell)\}^{\beta_{r,\ell}} \qquad (2)$$

Where $P(X_r[n-1] = \ell)$ is the probability of the module X_r being in state ℓ at time $n-1$, $0 \leq \alpha_{r,\ell} \leq 1$ and $0 < \beta_{r,\ell}$ are constants. Here, $f\{x\} = x$ if the influence is positive, otherwise $f\{x\} = 1 - f\{x\}$. Equation (2) is only the influence of state ℓ of module X_r on the transition probability $p_{ij}^{X_p}$ of the module X_p. Similar equations can also be written for influences of other states of all the modules, if any. These influences are called functional transitions in the SAN formulation [8]. We adopt *fading model* [7] to combine all the influences.

Thus, limiting probability, P_i of being in state i of the IGSMP model under the influence of other GSMP models is given as:

$$P_i^* = \frac{\pi_i^* \, \eta_i^*}{\sum_{j=0}^{N} \pi_j^* \, \eta_j^*}$$

where, π_i^* and η_i^* are limiting probability and sojourn time of the underline interacting model.

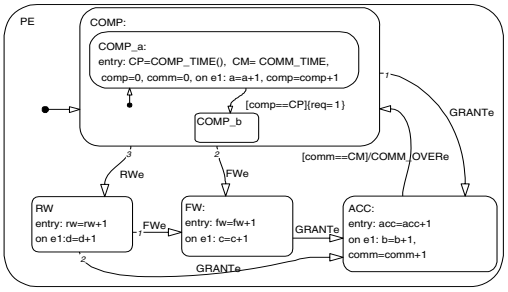

Figure 4. State structure of a PE.

4.2. Simulation methodology

In this section, we describe methodology to specify, simulate and analyze IGSMP model of a SSB architecture using various arbitration schemes in the Stateflow component of MATLAB [10].

We construct a library of generic blocks that can be combined in a bottom up fashion, to model communication architectures with fixed lottery and round robin arbitration policies. The generic building blocks model different types of resources in the system, e.g. PEs and arbiters with aforementioned arbitration policies. We instantiate building blocks from the library and integrate the system providing interfaces between blocks. This makes exploration of alternative arbitration schemes possible in lesser amount of time.

Figure 4 depicts generic building block showing state structure of a PE in the Stateflow. It has four states as explained in the Section 3. State *COMP* is the computing state of a PE, which lasts for random computing time

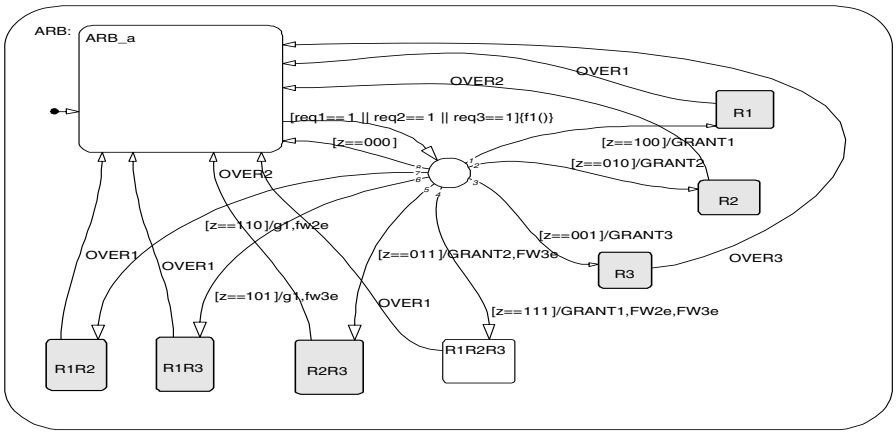

Figure 5. Simulink representation of fixed priority arbiter.

$\tilde{T}$. The syntax of the state consist of two major elements: the name of the state and various state actions (entry, during and exit state action and on event action). The state entry action of *COMP* state of all the PEs generates non-deterministic computing time $\tilde{T}$ and communication time $\tilde{C}$ in each communication transaction. For generation of $\tilde{T}$ and $\tilde{C}$, we invoke MATLAB m-function having predefined distribution, through graphical function *COMP_TIME()* and *COMM_TIME()*. A PE transits from *COMP* state to accessing state labelled as *ACC*, when arbiter generates *GRANTe* event. Arbiter model generates events viz. *GRANTe*, *FWe* and *RWe* depending on the priori status of the global system.

Similarly, we develop generic blocks for arbiters with different arbitration schemes. Generic building block of fixed priority arbiter in the Stateflow is shown in Fig. 5.

5. Results

We capture IGSMP model of SSB architecture with fixed, lottery based and round robin arbitration schemes in Stateflow component of MATLAB. An architecture has three PEs- PE_1, PE_2 and PE_3. In case of fixed arbitration scheme, we have assigned the highest priority to PE_1 and the lowest to PE_3. Input parameters to the model are- (i) random communication times of PEs viz. $\tilde{C_1}$, $\tilde{C_2}$ and $\tilde{C_3}$; and (ii) random computation times namely, $\tilde{T_1}$, $\tilde{T_2}$ and $\tilde{T_3}$. These times are generated by using MATLAB m-functions with generalized distribution. Simulation was performed on on P-IV, 1 GB Linux-workstation.

Various performance parameters of PEs viz. Band-Width (BW), Processing element Utilization (PU) and queue length at the memory ($\overline{L}$) have been estimated for aforementioned arbitration schemes. Table 1 shows results obtained through simulation of IGSMP model. The values shown are mean of parameters represented as percentages.

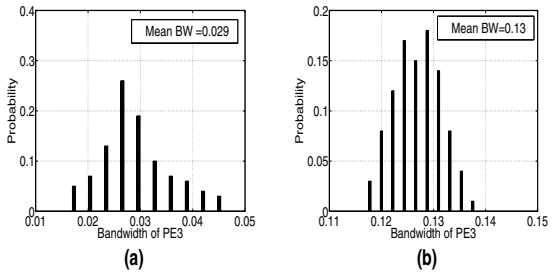

Figure 6. Pmf of BW of PE_3 for arbitration schemes (a) Fixed and (b) Round robin.

The columns denote performance metrics along with arbitration schemes, whereas rows list PEs. From the table following observations are made. (1) Memory bandwidth of PE_3, under fixed priority scheme is minimum at 8.43 %, being the lowest priority, while the highest priority PE_1 receives maximum bandwidth at 48.45 %, 5 times larger than PE_3. In column 4, we observe that bandwidth allocated in lottery arbitration scheme is better than fixed arbitration, except for top priority PEs of fixed priority arbitration scheme. Under round robin arbitration scheme, all PEs get guaranteed equal share of bandwidth. Moreover, maximum total bandwidth is only 42 % achieved in lottery based arbitration scheme as hence we infer that more PEs can be mapped to the bus to utilize idle time of the memory (58 %). Probability mass function (pmf) of bandwidth for PE_3 under fixed and round robin arbitration schemes are shown in Fig 6(a) and 6(b). Mean of bandwidth observed is 0.02 and 0.12 in two cases respectively. Similar results are obtained for PU

Table 1. Performance metrics comparison

	Fixed			Lottery			Round robin		
	BW (%)	PU (%)	$\overline{L}$ (%)	BW (%)	PU (%)	$\overline{L}$(%)	BW (%)	PU (%)	$\overline{L}$ (%)
PE_1	48.45	48.21	15.86	24.54	24.49	47.66	33.21	33.27	33.01
PE_2	43.29	43.32	21.99	42.47	42.51	23.89	33.27	33.43	32.79
PE_3	8.43	8.46	62.13	32.98	32.99	28.43	33.50	33.29	34.18

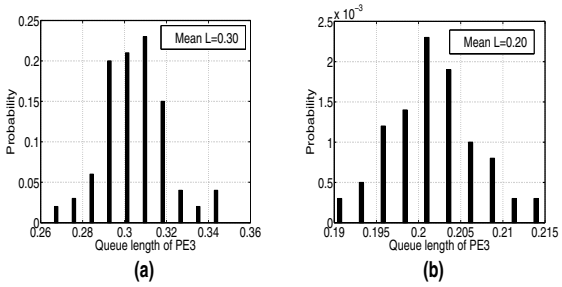

Figure 7. Pmf of $\overline{L}$ of PE_3 for arbitration schemes (a) Fixed and (b) Round robin.

also. (2) Queue length of PE_3 (62.13 %) in fixed arbitration scheme indicates that PE_3 spends comparatively more time in full and residual waiting states, before getting access to the memory. This is quite intuitive that, latency of lower priority masters is higher as compared to their high priority counterpart. In round robin arbitration scheme all PEs spend approximately equal amount of time in waiting states. Fig 7(a) and 7(b) depict pmf of queue length for PE_3 in fixed and round robin arbitration schemes, with mean observed 0.30 and 0.20 respectively.

6. Conclusions

The latency of arbitration is constant with round robin scheme whereas latency increases with decreasing priority of PEs in fixed arbitration scheme. The results demonstrate that the round robin arbitration scheme guarantees equal share of bandwidth allocation to all PEs as compared with fixed or lottery based arbitration scheme. However, these guaranteed share of bandwidth is achieved in round robin scheme at the cost of higher latency in case of high priority priority PEs of fixed arbitration scheme. Performance metrics of lottery based arbitration schemes are also comparable with those of round robin scheme, but not guaranteed. In case of fixed priority scheme, near starvation of lower priority components is observed. Starvation increases with decreasing priorities of PEs. Thus, round robin arbitration scheme offers an attractive alternative compared with other schemes considered here.

Acknowledgments

We gratefully acknowledge the financial support provided by the Department of IT, Ministry of Communication & IT, Govt. of India under SMDP-VLSI-II project.

References

[1] C. Asavathiratham, S. Roy, B. Lesieutre, and G. Verghese. The Influence Model. *IEEE Control System Magazine*, pages 52–64, December 2001.

[2] U. Deshmukh and V. Sahula. Stochastic modeling approaches for performance estimation of large electronic systems (VLSI systems). In *Int. Conf. on Special Functions and their Applications in Engineering*, 2007.

[3] S. Dey and S. Bommu. Performance analysis of a system of communicating processes. In *Proc. IEEE/ACM Int. Conf. on ICCAD*, pages 590–597, 1997.

[4] S. Kim, C. Im, and S.Ha. Schedule-aware performance estimation of communication architecture for efficient design space exploration. *IEEE Trans.on VLSI syst.*, 13(5):539–552, May 2005.

[5] K.Lahiri, A. Raghunathan, and S. Dey. System-level performance analysis for designing on-chip communication architecture. *IEEE Trans. on CAD of ICs & Syst.*, 20(6):768–783, June 2001.

[6] L.Benini and G.D.Micheli. Networks on chips: A new SoC paradigm. *IEEE Computer Magazine*, 35:70–78, Jan. 2002.

[7] M.R.Said, A. Oppenheim, and D. Lauffenburger. Modeling cellular signal processing using interacting Markov chains. In *IEEE Int. Conf. on ASSP*, pages 41–44, Apr. 2003.

[8] B. Plateau and K. Atif. Stochastic automata network for modeling parallel systems. *IEEE Trans. on Software Eng.*, 17(10):1093–1108, 1991.

[9] S.Pasricha, N.Dutt, and M.B.Romdhane. Using TLM for exploring bus based SoC communication architectures. In *Proc. Int. Conf. on ASAP*, 2005.

[10] Stateflow. MathWorks, Inc. (2007). [online]. available: http://www.mathworks. com/products/stateflow.

[11] T.Dumitras, S.Kerner, and R.Marculescu. Enabling on-chip diversity through architectural communication design. In *ASP-Design Automation Conf.*, pages 799–805, 2004.

[12] T.N.Mudge and H.B.Al-Sadoun. A semi Markov model for the performance of multiple-bus systems. *IEEE Trans on Computers*, C-34(10):768–783, Oct 1985.

[13] X. Zhu, W. Qin, and S. Malik. Modeling operation and microarchitecture concurrency for communication architectures with application to retargetable simulation. *IEEE Trans. on VLSI Syst.*, 14(7):707–716, July 2006.