Modeling and Synthesis of Molecular Memory

Renu Kumawat*
Department of Electronics & Communication Engg.
School of Electrical, Electronics & Communication
Manipal University Jaipur
Email: renukumawat@gmail.com*

Vineet Sahula† and Manoj Singh Gaur‡
†Department of Electronics & Communication Engg.
‡ Department of Computer Science & Engg.
Malaviya National Institute of Technology, Jaipur
Email: sahula@ieee.org†, gaurms@gmail.com‡

***Abstract*—Performance and reliability of nanoscale memory and logic devices is determined by few electron-phenomena. In this context, the organic molecules may offer some advantages for future memory applications. Since, a molecule is the smallest component whose electrical properties can be engineered, it can be argued that the ultimate integrated circuit will be constructed at the molecular level. This fact has been the driving force behind molecular electronics research of recent times. This article investigates the aspects of modeling, synthesis and analysis of nanocell based molecular memory. In our work, we have developed the HSPICE as well as probabilistic models for nanocell based molecular memory. An attempt has been made to develop a CAD tool for synthesis of such molecular memories which are posing interesting and promising research challenges at futuristic cutting edge of technology spectrum.**

***Index Terms*—Nanoscale, memory, molecular device, nanocell, molecules, uncertainty, transient errors.**

I. Introduction

Molecular electronics is emerging as one of the promising alternative to the beyond CMOS technology [1]. Such a device is fabricated using chemical self-assembly of mono or multiple layers of single or few, or array of molecules, to manifest the behavior of a wire, a switch or a latch. Researchers have demonstrated the switching behavior of these molecules and have fabricated simple logic functions as well as memory by using such programmable molecules. These bistable molecules form active molecular switches, which are used for bit storage in crossbar molecular memory. The area required for 1-bit storage is defined by diameter of the molecule and intersecting nanowires. Emerging molecular crossbar technology offers high density, regular array-like and non- volatile memory structure [2]. These devices consume low power, offer low programming voltage and high switching speed. Non-volatility feature provided by these molecular devices, permits memory to be used as programmable elements within a logic device with high density. However, the bottom-up approach employed for device fabrication at nanoscale lacks the precision in the molecular device ordering.

The programmable nanocell based approach mitigates this problem. In contrast to molecular crossbar devices, a nanocell [3], [4] consists of Gold Nanoparticles (GNPs) connected via randomly placed molecules and addressed by relatively small number of leads located at the edges. A self assembled monolayer of alkanethiols coats each nanoparticle and thus prevents them from coalescing into a multi-particle array. The electrical contacts are established via metal-molecule chemical bonding. These molecules exhibit re-programmable negative differential resistance (NDR) characteristics and show hysteresis. However, the characteristics of single or few molecular devices are extremely sensitive to the external parameters such as contacts, nanogap, environment, etc. Such a sensitivity poses a serious design challenge to realize the reliable molecular devices. In contrast to other molecular devices, a nanocell consists of conducting metal nanoparticles connected via self assembled monolayer of molecules. Tour et *al.* demonstrated that the nanocell device has an in-built defect tolerance, ultra high density, post fabrication programmability through mortal training and hence lack the need for precise molecular ordering. These features makes nanocell a good choice for future nano-scale devices.

II. Proposed Work

One of the primary goals is to illustrate modeling and post fabrication synthesis algorithm for a nanocell based molecular memory device [5]. Also, we have analytically proved that such a memory can withstand environmental uncertainties [6]. A model building is demonstrated and extended over an already proposed analytical framework for molecular devices [7]. The model is based on circuit behavior of nitro-substituted Oligo (Phynylene Ethynylene) (OPE) molecule [8]. This model is subsequently used to simulate crossbar molecular devices as well as nanocell based 1-bit molecular memory and verified using HSPICE. Due to hysteresis characteristics of OPE molecule, it is observed that even an untrained nanocell behaves as 1-bit memory cell. The proposed nanocell molecular memory demonstrates read, write and erase capability. The concept is further augmented by post fabrication synthesis of 2-bit molecular memory using external control signal voltages. Most suitable high and low voltage values for these control signals is a design space search problem. This search is handled by Genetic Algorithm such that some of the molecules turn to $'ON'$ or $'OFF'$ state and the nanocell is programmed to behave as a 2-bit memory cell [5].

978-1-4799-1743-3/15/$31.00

Further, a computational framework is proposed to compute the probability of retrieving the stored data bits correctly at the output terminal of the proposed nanocell. A novel extension over the continuous parameter birth-death model is also proposed to estimate the reliability of a nanocell, in presence of transient errors [6]. In this computational framework, the steady state probability and probability of being in each substate is computed. The proposed approach is augmented to theoretically determine the expected lifetime and availability of the nanocell using the birth-death model of molecules and their spatial connectivity. The lower and upper bounds for nanocell reliability are calculated. Algorithms are developed and implemented in MATLAB, PERL and HSPICE to (i) generate an instance of nanocell consisting of N nanoparticles (ii) compute the probability that at least one path is present between input and output node of nanocell (iii) bounds on reliability of the nanocell (iv) automatically generate the proposed model representation for a given nanocell and use it to estimate the $success\_ratio$ as well as the nanocell reliability, while considering the uncertainties. Theoretical results for reliability estimations are validated by simulating HSPICE model of nanocell in presence of varying defect rates.

Our Contributions:

1) During exploration, this nanocell configuration is simulated by systematically varying the number of nanoparticles and molecular switches. It is observed that, the probability of existence of at least one path, from input to output, approaches close to unity with presence of at least 20 or more nanoparticles in the nanocell.
2) During memory model validation, 1000 samples of 1-bit memory (consisting of 20 nanoparticles) are generated using Monte Carlo simulation and verified for read and write operations. It is observed that such a memory cell can successfully perform read and write operations for more than 99.5% of the untrained nanocell based 1-bit memory samples.
3) It is observed that to successfully train a 2-bit molecular memory, the number of control signals should be more than approximately one-fourth of total number of nanoparticles.
4) Our results demonstrate that the proposed methodology is versatile enough to train nanocell for multi-bit storage functionality.
5) It is observed that as long as, molecular failure rate is less than its repair rate, the nanocell functions correctly. Also, the device reliability increases with increase in the number of nanoparticles and molecules which is validated by theoretical formulation.

III. Conclusion and Future Work

The molecular memory design and synthesis is viewed as a long term research goal. In our work, we have developed the HSPICE as well as probabilistic models for nanocell molecular memory. An attempt has been made to develop a CAD tool for synthesis of such molecular memories. The proposed methodology is flexible enough to design multibit memory and logic device. Although, the problem of nanocell molecular memory modeling, synthesis and analysis has been thoroughly explored, there are still some potential improvements that should be explored.

Genetic Algorithm consumes large amount of time for convergence, even for training a small nanocell of 50 nanoparticles. Thus, adaptive learning algorithms need to be explored to reduce the training time. Another promising direction can be to augment the proposed nanocell model by including the power and delay modeling issues. Also, the fault model for the nanocell must be proposed and used for molecular memory testing. The proposed hybrid CMOS-NANOCELL architecture needs to be realized. Again the issues related to connecting the two nanocells together must be addressed in near future. Although, the present CMOS read/write circuitry can be used for the proposed nanocell molecular memory, the nano-scale read/write circuitry must be proposed and realized. Further, the extension of proposed model which considers the aging effects is under progress and is part of future work. Such a model can be used for estimating data retention time of nanocell memory. Moreover, in future, we plan to validate the mathematical framework by fabricated nanocell, in presence of environmental uncertainties and aging effects.

References

[1] "International technology roadmap for semiconductors," 2013. [Online]. Available: http://itrs.net

[2] J. E. Green, J. Wook Choi, A. Boukai, Y. Bunimovich, E. Johnston-Halperin, E. DeIonno, Y. Luo, B. A. Sheriff, K. Xu, Y. Shik Shin, H.-R. Tseng, J. F. Stoddart, and J. R. Heath, "A 160-kilobit molecular electronic memory patterned at 10^{11} bits per square centimeter," *Nature*, vol. 445, pp. 414–417, 2007/01/25/print. [Online]. Available: http://dx.doi.org/10.1038/nature05462

[3] C. Husband, S. Husband, J. Daniels, and J. Tour, "Logic and memory with nanocell circuits," *IEEE Transactions on Electronic Devices*, vol. 50, no. 9, pp. 1865 – 1875, sep 2003.

[4] J. Tour, W. Van Zandt, C. Husband, S. Husband, L. Wilson, P. Franzon, and D. Nackashi, "Nanocell logic gates for molecular computing," *IEEE Transactions on Nanotechnology*, vol. 1, no. 2, pp. 100 – 109, jun 2002.

[5] R. Kumawat, V. Sahula, and M. S. Gaur, "Probabilistic modeling and analysis of molecular memory," *J. Emerg. Technol. Comput. Syst.*, vol. 11, no. 1, pp. 6:1–6:16, Oct. 2014. [Online]. Available: http://doi.acm.org/10.1145/2629533

[6] ——, "A probabilistic model for nanocell reliability evaluation in presence of transient errors," *IET Computers Digital Techniques*, vol. 9, pp. 213–220, July 2015.

[7] G. Rose, Y. Yuxing, J. M. T., C. C. Adam, G. Nadine, M. Nabanita, C. B. John, R. H. Lloyd, and R. S. Mircea, "Designing cmos/molecular memories while considering device parameter variations," *ACM Journal on Emerging Technologies in Computing Systems (JETC)*, vol. 3, no. 1, 2007.

[8] H. Kim, S. S. Jang, R. A. Kiehl, and W. A. Goddard, "Negative differential resistance of oligo(phenylene ethynylene) self-assembled monolayer systems: The electric-field-induced conformational change mechanism," *The Journal of Physical Chemistry C*, vol. 115, no. 9, pp. 3722–3730, 2011. [Online]. Available: http://pubs.acs.org/doi/abs/10.1021/jp1114916