Design and Fabrication of Si-Diaphragm, ZnO Piezoelectric Film-Based MEMS Acoustic Sensor Using SOI wafers

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***Abstract*—This paper reports a simpler technique for fabricating an microelectromechanical system acoustic sensor based on a piezoelectric zinc oxide (ZnO) thin film, utilizing silicon-on-insulator wafers. A highly *c*-axis-oriented ZnO film of thickness 2.4 μm, which is covered with 0.2-μm-thick PECVD SiO_2, is sandwiched between two aluminum electrodes on a 25-μm-thick silicon diaphragm. This diaphragm thickness has been optimized to withstand sound pressure level range of 120–160 dB. Stress distribution studies using ANSYS have been performed to determine the locations for placement of capacitor electrodes. This paper also reports a technique for the creation of a positive slope of the ZnO step to ensure proper coverage during Al metallization. In order to maximize yield, process steps have been developed to avoid the microtunnel blockage by silicon/glass particles. The packaged sensor is found to exhibit a sensitivity of 382 μV/Pa (RMS) in the frequency range from 30 to 8000 Hz, under varying acoustic pressure.**

***Index Terms*—Diaphragm, silicon-on-insulator (SOI) substrate, sound pressure level (SPL), thin film, zinc oxide (ZnO) film.**

I. Introduction

THE FIRST piezoelectric material-based microphone was presented by Royer *et al.* [1]. They used ZnO film of thickness 3–5 μm on 30 μm-thick silicon diaphragm. A sensitivity of 50–250 μV/Pa was achieved in the frequency range 10 Hz to 10 kHz. The application of silicon micromachining for fabrication of microphones has been reported resulting in small size piezoelectric, piezoresistive and capacitive microphones [2]. A piezoelectric ZnO-based high-Q single-crystal silicon (SCS) resonator has been presented in [3].They have used zinc oxide because of its well-established process recipe and ease of integration with current microelectronics. Other authors have also presented the piezoelectric ZnO-based microphones and acoustic devices [4]–[9], facilitated by excellent compatibility of ZnO with the CMOS process. However, in all of these papers, the fabrication process does not use SOI wafers. Further, the membrane material is one of the following: silicon-silicon dioxide, silicon nitride, silicon dioxide-silicon nitride with thickness 9.5 μm to 0.5μm, 1.0 μm to 1.5 μm, 0.2 μm to 1.7 μm respectively. The sensors have been designed for different applications such as hearing aid, microphone cum microspeaker and underwater studies. The acoustic sensor reported in the present paper differs from those reported in the aforesaid papers in terms of membrane thickness, fabrication process (use of SOI wafer, ZnO etching by electrolytically-added copper ions and microtunnel), application for higher SPL range (120–160 dB) and wide bandwidth (30–8000 Hz). Development of this sensor required special considerations in design and fabrication.

Besides ZnO, other piezoelectric materials such as lead zirconate titanate (PZT), PVDF, $PbTiO_3$, $LiNbO_3$ crystals, and AlN have also been used. However, the compatibility of these materials with CMOS process has always been an issue. Some authors have presented the PZT-based ultrasonic transducer [10]–[13], acoustic sensor [14], [15], high sensitivity pressure microsensor [16] and accelerometers [17], [18]. The PZT-based acoustic sensor exhibits lower sensitivity [14] in comparison to ZnO based sensor because, for instance, the relative dielectric constant of PZT is more than 100 times that of ZnO, so the capacitance of PZT-based sensor is at least 100 times that of ZnO based ones with same dimensions. ZnO film is most widely used as a piezoelectric material because of its excellent piezoelectric and dielectric properties. This film has been used in the field of MEMS, with both surface micromachining [19] and bulk-micromachining [20], due to its good piezoelectric performance and excellent bonding on various materials.

A ZnO-based MEMS acoustic sensor of sensitivity, 300 μV/Pa was described in [20]. The approach of the present work differs in the following respects: (1) The device in [20] was fabricated on planar silicon wafer instead of SOI wafer causing non-uniformity of diaphragm thickness, (2) the ZnO etching was done using HCl solution which produces negative edge slope of ZnO, leading to step-coverage problems and resulting in Al film breakage over the step accompanied by device failure during vibration testing, (3) fabrication of microtunnel was done by LOCOS process which increases the number of fabrication steps and also process complexity, (4) anodic bonding of silicon on pyrex glass wafer was done after ZnO deposition degrading ZnO film during subsequent processing, (5) silicon-glass dicing was done using single spindle which led to microtunnel blockage.

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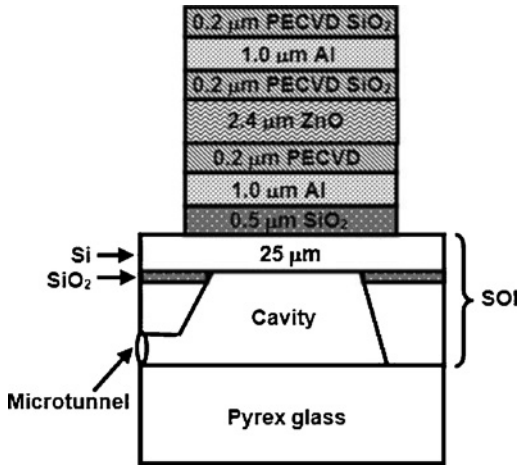


Fig. 1. Cross-sectional view of the MEMS acoustic sensor.

To overcome all of the above problems, the present approach developed a new process for fabrication of acoustic sensor using SOI wafers. The main motive behind using SOI wafers is that the buried silicon dioxide layer acts as an etch stop for tetra methyl ammonium hydroxide (TMAH) solution, which has a good selectivity of Si over SiO_2. Moreover, the process ensures uniformity of diaphragm thickness. A correctional view of the device is shown in Fig. 1. The paper is organized as follows. We elaborate design and simulation of structure in Section II. The process steps for fabrication are illustrated in Section III, with discussion of results obtained in Section IV. We conclude in Section V.

II. Simulation and Design

A. Diaphragm and Microtunnel Design

In load deflection technique, the deflection of suspended film is measured as a function of applied pressure. The load-deflection relationship of a flat square diaphragm [21] is given by (1).

$$\frac{Pa^4}{Eh^4} = \frac{4.2}{\left(1-v^2\right)}\left[\frac{y}{h}\right] + \frac{1.58}{(1-v)}\left[\frac{y}{h}\right]^2 \tag{1}$$

Where P is applied pressure (Pascal), y is deflection from the center of diaphragm, a is half of side length, h is the diaphragm thickness, E is Young's modulus and v is Poisson's ratio of diaphragm material. As obtained in (1), the deflection range may be divided into two regions: the first term of right-hand side, describing the linear region (deflection less than 25% of the diaphragm thickness) and second term (i.e., cubic term) describing the non-linear region. For the linear part, we have

$$y = \frac{Pa^4\left(1-v^2\right)}{4.2Eh^3} \tag{2}$$

For silicon diaphragm of size 3 mm × 3 mm, the thickness has been optimized within sound pressure level (SPL) range of 120–160 dB using (2). The deflection at the center of the silicon diaphragm with different sound pressure levels has been plotted in Fig. 2(a). The values of E and v for silicon have been given in Table I. In the SPL range 120–160 dB, for all the three diaphragm thicknesses (20, 25, 30 μm), the deflection is less than 25% of the corresponding thickness. Hence, all the three diaphragm thicknesses can provide linear output. At 180 dB, the deflections in 20, 25, 30 μm-thick diaphragms are 20.5, 10.5, 6.0 μm, respectively; whereas at 160 dB, the deflections are 2.0, 1.0 and 0.6 μm, respectively. For safety of diaphragm, the 20 μm-thick diaphragm is unsuitable because it gives very large deflection at 180 dB. Since the 30 μm-thick diaphragm gives very small deflection at 160 dB, the 25 μm-thick diaphragm has been selected for SPL range 120–160 dB to operate the device in linear region with optimum sensitivity.

Calculation of resonance frequency of diaphragm (25 μm-thick silicon and 0.5 μm-thick SiO_2 layer) is essential to ensure that the device will work in linear region. For this purpose harmonic analysis has been performed using ANSYS using the material properties as given in Table I and the element type SOLID-45. The variation of deflection with frequency is plotted in Fig. 2(b) at an arbitrary applied pressure of

TABLE I
Material Properties Used in Simulation

Material	Young's Modulus (GPa)	Poisson's Ratio	Density (kg/m^3)
SiO_2	65	0.17	2648
Si	135	0.28	2330

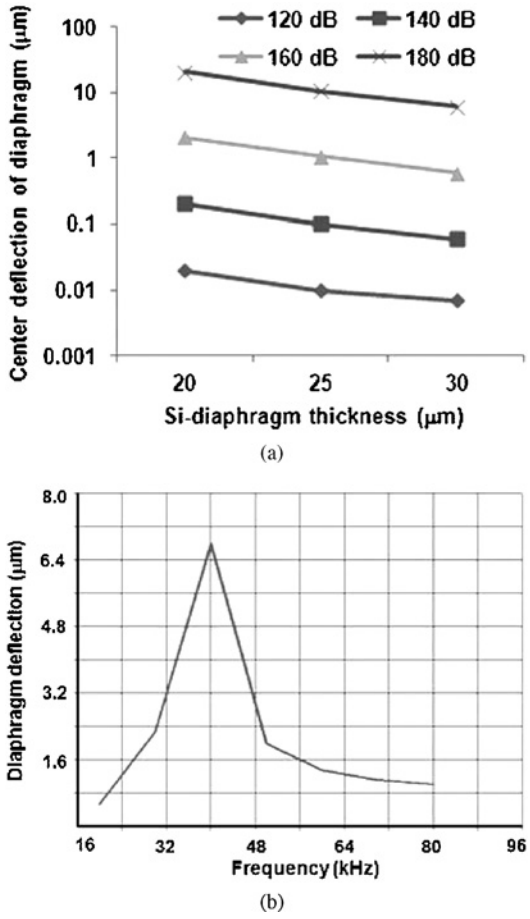


Fig. 2. (a) Relationship between deflection and thickness of silicon diaphragm at different sound pressure levels. (b) Variation of deflection at center of diaphragm with frequency (ANSYS plot by harmonic analysis).

400 Pascal. It is found that the deflection is maximum at 40 kHz. Thus, the resonance frequency of the diaphragm is 40 kHz. Below 16 kHz the deflection is small. As the designed acoustic sensor has to operate from 30–8000 Hz which is sufficiently far away from the resonance frequency, it is expected the sensor will have a flat response, which will be experimentally verified after fabrication in Section-IV.

Finite element modeling by ANSYS has been performed to study the stress distribution of square diaphragm. The static analysis has been done using element type SOLID-45 to obtain the stress distribution under uniform pressure load (400 Pa), as shown in Fig. 3(a). The edges of the diaphragm were clamped and this condition was applied as boundary condition in the simulation. It was observed that the maximum stress was generated at the center and a part of edges of square diaphragm. To get the maximum sensitivity of the device, this result gives the location for fabricating the two sets of parallel electrodes, one around the center and another near the edges of the diaphragm. Taking these results into consideration, two capacitors, one on center and another on the outer edge of the diaphragm have been designed. The capacitor designed on center of the diaphragm has the value 82 pF, whereas the capacitor on outer edge of the diaphragm has the value 145 pF. The thickness and dielectric constant of ZnO layer were taken as 2.44 μm and 11.8 respectively. Thickness and dielectric constant of PECVD SiO_2 layers were taken as 0.2 μm and 3.18 respectively.

Cavity and microtunnel design determine the lower cut-off frequency of the device. A cavity filled with air stores potential energy while the gas is compressed. Therefore, the cavity in the structure (Fig. 1) is modeled as acoustic compliance. The value of this compliance [22] is given by (3)

$$C_{cav} = \frac{V_{cav}}{\rho_{air} c^2} \tag{3}$$

Here, C_{cav} is cavity compliance, V_{cav} is cavity volume and c is the speed of sound.

The microtunnel is used to equilibrate the vent to the ambient pressure. Assuming the flow of air in microtunnel as fully developed laminar flow, the acoustic resistance through the microtunnel (vent) [23] is given by (4), where μ_{air} is viscosity of air, L_{eff} is the effective microtunnel length, and D_{vent} is hydraulic diameter of microtunnel.

$$R_a = \frac{128 \mu_{air} L_{eff}}{\pi (D_{vent})^4} \tag{4}$$

The hydraulic diameter is given by (5), where L is the length and W is the width of rectangular opening of microtunnel.

$$D_{vent} = \frac{2LW}{2(L+W)} \tag{5}$$

In the present design, $V_{cav} = 3420 \times 10^{-12} m^3$, $L_{eff} = 11833\,\mu$m, $L = 100\,\mu$m and $W = 35.0\,\mu$m were taken. The value of D_{vent} is calculated from (5) and found to be 51.8 μm. By putting these values in (3) and (4), C_{cav} and R_a were calculated and found to be $2.41 \times 10^{-14} m^5/N$ and $1.24 \times 10^{12} Ns/m^5$, respectively. The lower cut-off frequency is given by (6).

$$f_c = \frac{1}{2\pi R_a C_{cav}} \tag{6}$$

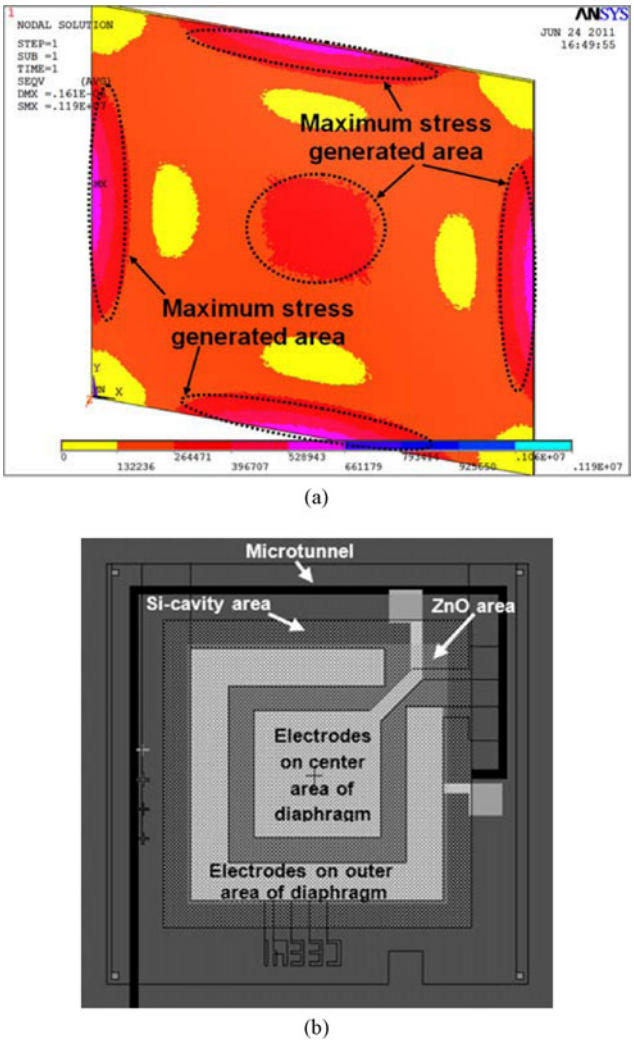


Fig. 3. (a) ANSYS simulation results of stress distribution in a square diaphragm. (b) Mask layout of acoustic chip.

By putting the values of cavity compliance (C_{cav}) and microtunnel resistance (R_a) in (6), the value of f_c is calculated as 5.3 Hz.

B. Mask Layout

The top view of the six-level mask designed using L-Edit is shown in Fig. 3(b). Mask#1 for acoustic microtunnel; Mask#2 for silicon diaphragm; Mask#3 for bottom electrodes; Mask#4 for ZnO patterning; Mask#5 for top electrodes and Mask#6 for pad opening have been designed for device fabrication. In [20], the tunnel is slightly penetrating the diaphragm area whereas in proposed design, the tunnel structure end at the edge boundary of the diaphragm. This does not make the alignment critical because lateral etching of silicon in TMAH is sufficient to open the tunnel to the cavity.

C. Sensitivity

The sensitivity of the piezoelectric based device as given in [15] is reproduced in (7), where A_{piezo} denotes the area of piezoelectric layer; σ, the applied stress; d_{31}, the trans-

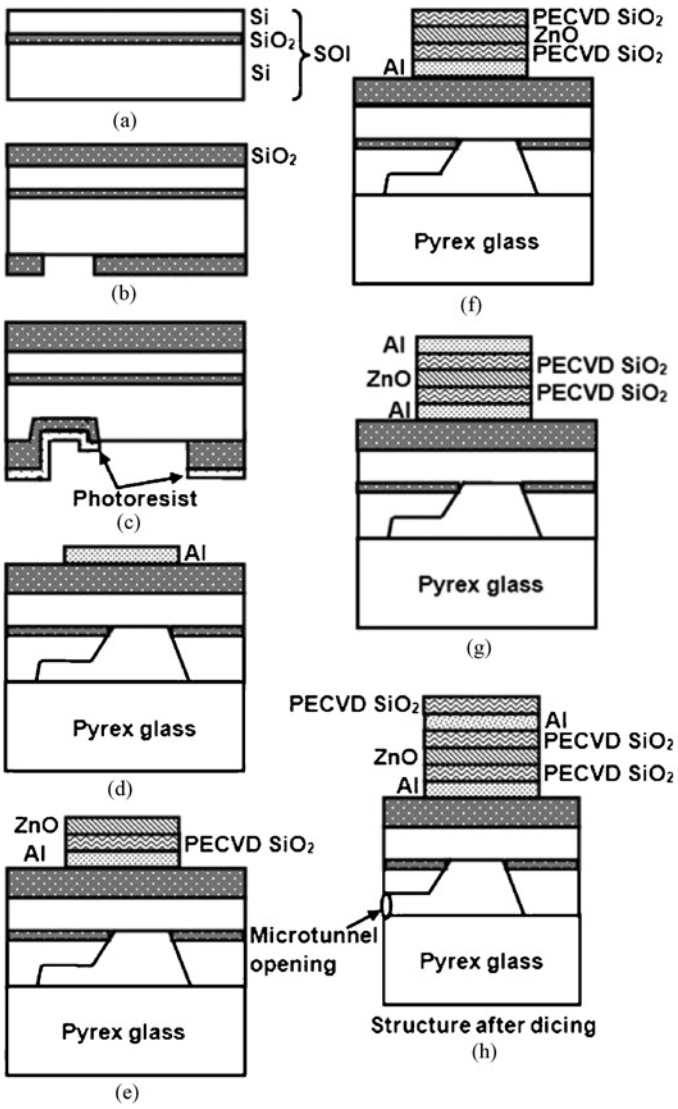


Fig. 4. Fabrication steps for device. (a) Selection of SOI wafer. (b) Thermal oxidation and microtunnel pattering (mask#1). (c) Microtunnel etching, thermal oxidation, and diaphragm patterning (mask#2). (d) Cavity etching for diaphragm, anodic bonding, Al deposition, and patterning (mask#3). (e) PECVD SiO_2 deposition, ZnO deposition, and patterning (mask#4). (f) PECVD SiO_2 deposition. (g) Al deposition and patterning (mask#5). (h) PECVD SiO_2 deposition, pad opening (mask#6), and dicing.

verse piezoelectric coefficient; C_{load}, the load capacitance; and C_{piezo}, the capacitance of piezoelectric layer.

$$Sensitivity = \frac{A_{piezo}\sigma d_{31}}{C_{load} + C_{piezo}} \tag{7}$$

The value of piezoelectric coefficient of piezoelectric layer increases with the thickness of the layer up to 2.5 μm [24]. After this thickness, the value of piezoelectric coefficient is saturated. If the thickness increases beyond this value, the total thickness of the diaphragm gets increased. As a result, at a fixed pressure, the diaphragm deflection decreases. Since, the voltage of the acoustic device is directly proportional to the deflection of the diaphragm [24], therefore the sensitivity of the device decreases. Also experimentally, it has been shown that the thinner film has better sensitivity [6].

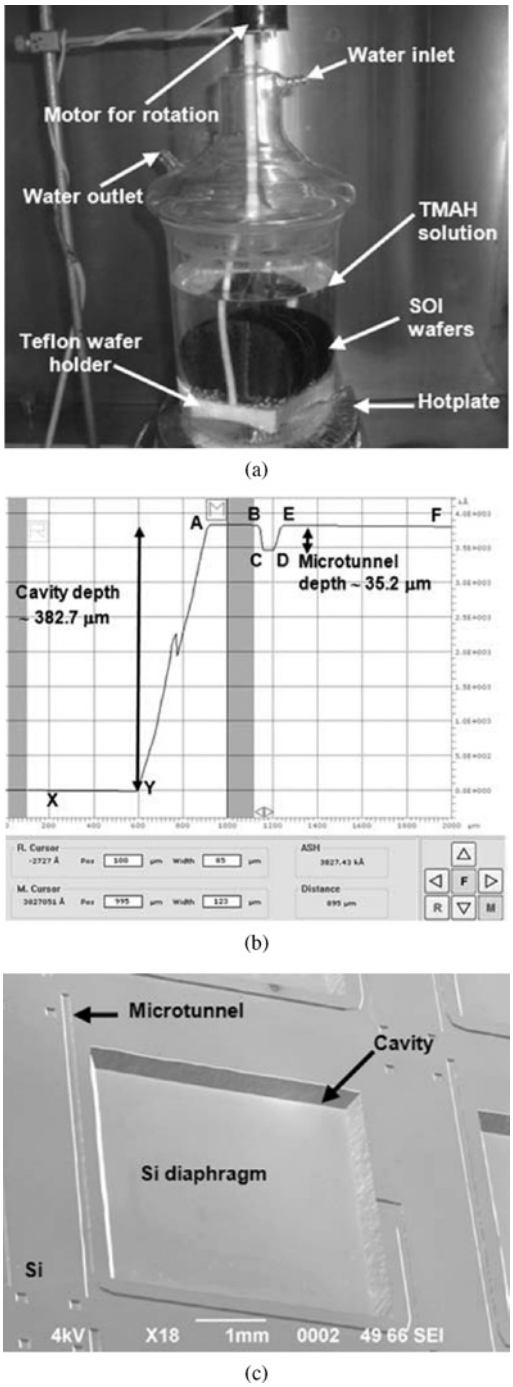


Fig. 5. (a) Experimental setup for bulk micromachining. (b) Cavity depth measured using Dektak 6 M surface profiler. (c) SEM photograph of backside of structure after bulk micromachining.

III. Fabrication

Process sequence for fabrication of acoustic sensor is shown in Fig. 4. The fabrication of acoustic sensor was started with 4-inch diameter SOI wafers with 25 μm-thick active layer. The resistivity and thickness of buried SiO_2 layers of these wafers were 10–20 Ω.cm and 1.0 μm respectively. The fabrication of acoustic sensor was carried out with six masks. RCA1 and RCA2 cleaning of these wafers were done by making the solution of deionized water (DI), NH_4OH, H_2O_2 in a ratio of 5:3:3 and DI water, HCl, H_2O_2 in same ratio respectively.

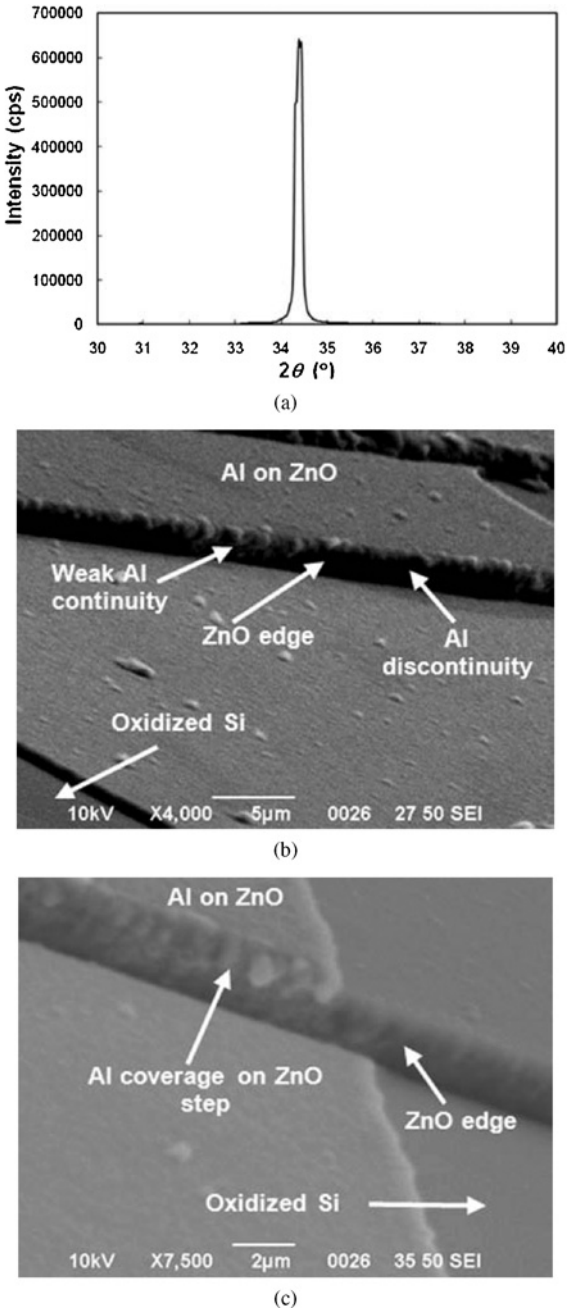


Fig. 6. (a) XRD pattern of a 2.4-μm-thick ZnO film. (b) SEM image of structure after etching in the HCl solution. (c) SEM image of structure after etching in the NH_4Cl solution.

The 0.5 μm-thick SiO_2 layer was thermally grown at 1000 °C. Photolithography (Mask#1) for microtunnel was performed using positive photoresist S1818.

A. Bulk-Micromachining of Si for Microtunnel

After removing SiO_2 layer using BHF from microtunnel area, wafers were subjected to bulk-micromachining of Si in 25% TMAH at 65 °C. The experimental setup of TMAH etching is shown in Fig. 5(a). For uniform silicon etching, wafers were rotated at 5 RPM in the solution. A smooth microtunnel of approximately 100 μm width was successfully etched. Depth of microtunnel was measured using Dektak 6 M surface profiler. In Fig. 5(b), the stylus of surface profiler moves from point A to B on top flat silicon surface. From point B to C, it goes down into the microtunnel and then travels from point C to D on the bottom surface of microtunnel. It starts climbing up the microtunnel wall from point D to E and ends at point F. The average step height (ASH) from point B to C or D to E is measured as microtunnel depth = 35.2 μm.

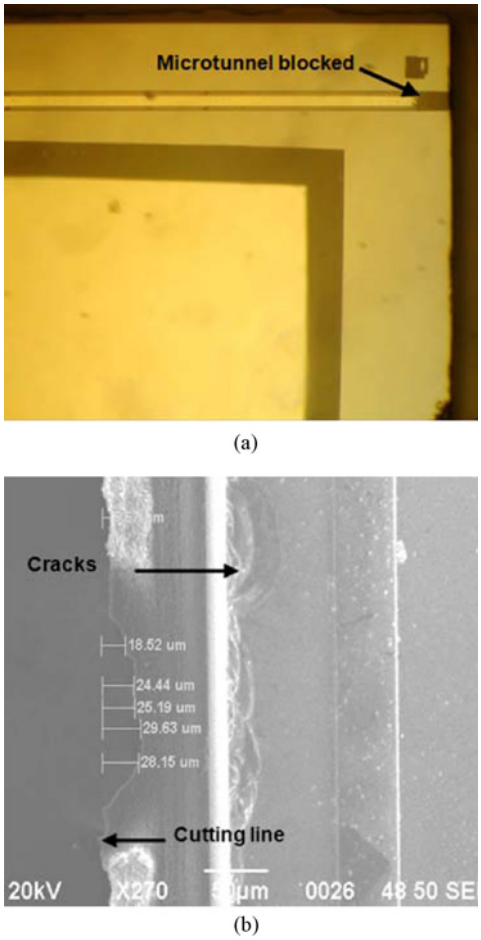
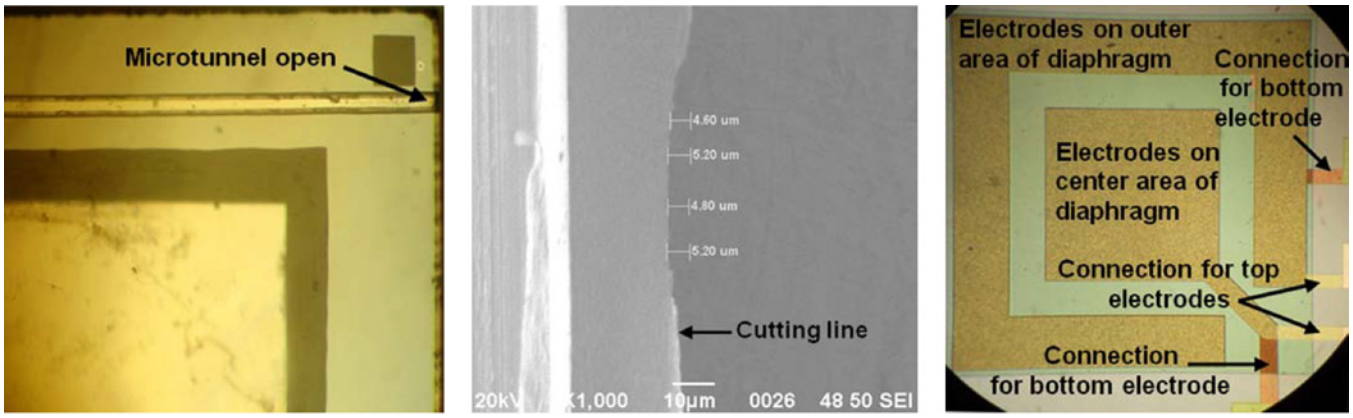


Fig. 7. Photograph of structure after dicing. (a) Microtunnel blockage. (b) Chipping in edge of acoustic chip.

B. Bulk-Micromachining of Si for Diaphragm

In order to fabricate a 25.0 μm-thick silicon diaphragm, thermal oxidation was done after microtunnel etching. Thickness of SiO_2 was measured using Dektak 6 M surface profiler, and found to be 1.2 μm. Photolithography (Mask#2) for defining diaphragm area was performed using negative photoresist SU8–2025. Microtunnel of 35.2 μm depth and 100 μm width, was completely covered with SU8 during oxide etching. After piranha cleaning, bulk-micromachining of silicon was done using 25% TMAH solution at 70 °C for 33 hours approximately. The silicon etching was automatically stopped at buried oxide layer of SOI wafer. The cavity depth was measured using Dektak 6 M surface profiler. As shown in Fig. 5(b), the stylus moves from the point X at the bottom flat surface of the cavity, climbing up the cavity wall from the point Y and ends at point A on top flat surface. Thus, average step height (ASH) or cavity depth is measured = 382.7 μm. The 25 μm-thick silicon



(a) (b) (c)

Fig. 8. Photographs of structure after dicing. (a) Microtunnel open at the chip edge. (b) Chipping in edge of acoustic chip. (c) Front view of fabricated chip.

TABLE II
PARAMETERS USED IN DICING

Dicing Parameters	In Case of Blocked Microtunnel, Spindle Z_1 on, But Spindle Z_2 Off	In Case of Open Microtunnel, Both Spindles Z_1 and Z_2 were on
Blade cooler (L/min)	0.8	0.5
Shower (L/min)	1.0	1.5
Spray (L/min)	1.0	0.5
Feed speed (mm/s)	10	1.0
Spindle speed (rpm)	30 000	20 000

TABLE III
COMPARISON OF PRESENT WORK WITH [20]

Process Novelties and Results	Present Work	Previous Work [20]
Type of silicon wafer used	SOI	Planar Si
Diaphragm thickness uniformity (μm)	25.0 $\pm$ 0.5	25.0 $\pm$ 5.0
ZnO etchant used	20% NH_4Cl	0.25 % HCl
Al step coverage	Good	Poor
Dicing method	Using two spindles	Using single spindle
Chipping (μm)	$<$ 5.2	18–28
Microtunnel blockage	10%	Mostly
Number of process steps	11	15
Fabrication yield	High $\sim$80%	Low
Sensitivity (μV/Pa)	382–191	150–300

diaphragm was fabricated on SOI wafer using new technique. A smooth microtunnel opening in deep cavity is shown in Fig. 5(c). Lateral etching of silicon in TMAH is sufficient to open the microtunnel to the cavity, and it does not make the alignment critical with diaphragm boundary.

C. Anodic Bonding

Silicon dioxide layer was completely removed from the backside of these wafers for anodic bonding. To seal the cavity, anodic bonding was done using EVG-520 bonder at 600 V. The bonding parameters were as follows: temperature = 330 °C, voltage = 600 V, vacuum = 5×10^{-3} mbar and bonding time = 20 minutes. In this process, 4-inch pyrex glass wafer was used.

D. Fabrication of Structure on Front Side of the Glass-Bonded Wafer

On front side of bonded wafer, two pairs of electrodes, one near the edge and another in the center of the diaphragm were fabricated. For this purpose, 1.0 μm-thick aluminum (Al) was deposited using sputtering technique. Photolithography (Mask#3) was performed for patterning the bottom electrode. After Al etching, 0.2 μm-thick SiO_2 layer were deposited using PECVD technique followed by deposition of 2.4 μm-thick ZnO layer using RF magnetron sputtering (with following environmental parameters; power = 500 W, gas composition = 40% Ar + 60% O_2, pressure = 20 mtorr and deposition rate = 0.6 μm/hr). XRD pattern of deposited ZnO thin film on a bare silicon wafer is shown in Fig. 6(a). It was observed that the growth of the film is highly oriented along c-axis normal to the substrate because there is only one peak corresponding to (002) reflection of wurtzite phase of ZnO. At an angle of 2θ = 34.4°, the ZnO film exhibits a strong peak, which indicates that the ZnO film grains have good orientation. This result is similar to that obtained in [20, 25]. Photolithography (Mask#4) for patterning ZnO film was performed using positive photoresist S1818. The etching of ZnO layer was done using

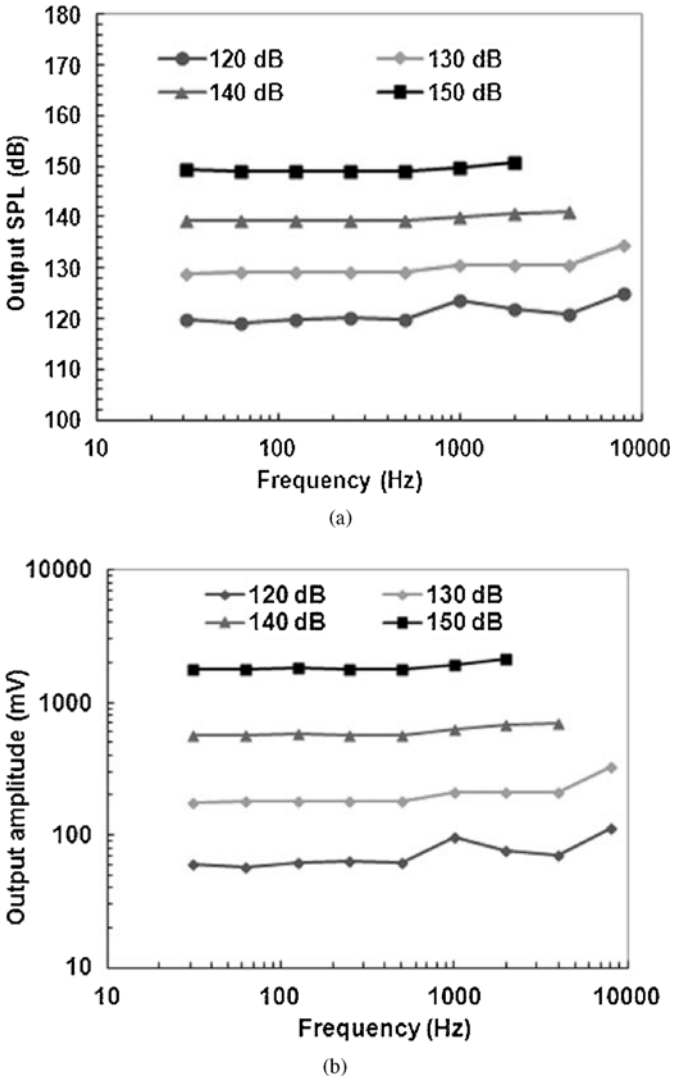


Fig. 9. (a) Frequency response of a packaged acoustic sensor as a function of input SPL. (b) Output response of the sensor as a function of SPL.

20% NH_4Cl solution with electrolytically-added copper ions [26]. SEM photographs in case of earlier technique (etching in HCl solution) and proposed technique (etching in NH_4Cl solution) after Al deposition, are shown in Fig. 6(b) and 6(c) respectively. It was observed that Al did not cover the ZnO step at many locations in case of HCl solution whereas Al coverage on ZnO step was much better in case of NH_4Cl. The PECVD SiO_2 of 0.2 μm thickness was again deposited for passivation.

E. Dicing of Fabricated Glass-Bonded Wafer

Microtunnel of each device was opened during dicing. The dicing parameters play an important role in the yield of the devices. The two sets of dicing conditions were chosen, as given in Table II. In the first case, only single spindle was used. The diamond blade of 200 μm thickness, is used to cut the silicon wafer and then glass. The stage speed was kept at 10 mm/min. The spindle speed was kept at 30,000 RPM. When dicing was completed in this sequence, several microtunnels were blocked by the silicon/glass particles, [as shown in Fig. 7(a)], created by damages caused by chipping at the edges of the devices [Fig. 7(b)]. Cracks are clearly seen in the SEM picture of Fig. 7(b). Large chipping, 18–28 μm was observed in this case. As there existed a vacuum inside the microtunnels after anodic bonding, the particles were sucked into them as soon as they were opened by dicing. These microtunnels could not be opened easily because it was not possible to subject the devices to any acid cleaning procedure at this stage. In the second case, two spindles were used, one for cutting glass and the other for silicon. The diamond blade of 200 μm thickness, was used to cut glass wafer first and then a 100 μm-thick blade to cut the silicon wafer. The stage and spindle speeds were kept as 1 mm/sec and 20,000 RPM respectively. This way the silicon wafer was not damaged by the 200 μm-thick blade, reducing the microtunnel blockage problems and chipping, as shown in Fig. 8(a) and (b) respectively. The front view of fabricated acoustic sensor after dicing using proposed technique is shown in Fig. 8(c). Together with the slower stage and spindle speeds, a good surface finish was achieved, as shown in the SEM photograph of Fig. 8(b). Maximum chipping of 5 μm was observed in this case. Different combinations of stage and spindle speeds were tried but the above combination gave the best results.

A few process runs were also carried out separately with planar silicon wafers. But these wafers needed to be repeatedly checked with surface profiler to determine the silicon thickness etched. Also, there was a wide variation in the depth of the cavity after TMAH etching over the 4-inch diameter wafer. Therefore, experiments with planar silicon wafers were discontinued. This study established that the SOI process might be essential for fabrication of this device to ensure higher yield.

IV. Results and Discussion

The microtunnel allows the flow of air in and out of the cavity to compensate the pressure applied on the diaphragm. The actual output of the sensor is obtained at desired frequency due to the resistance offered by microtunnel while the air flows through it. The deflection in the diaphragm due to acoustic pressure generates the lateral stress in the ZnO layer, which in turn converts it into transverse polarization. The performance of packaged acoustic devices has been tested over a wide frequency range of 30–8000 Hz at different sound pressure levels (SPL) 120–160 dB. The measured values of capacitance of the devices at the center and at the periphery of the diaphragm were obtained as 83.8 pF and 139.8 pF, respectively [using a Precision LCR Meter 4284A from Agilent]. The corresponding loss tangents were found to be 0.004 and 0.003, respectively. The frequency response of packaged acoustic sensor has been studied at different input SPL, and illustrated in Fig. 9(a). It was observed that the output increases linearly with increase in the input SPL over the range 120–150 dB in frequency range 30–8000 Hz. The output response of the sensor as a function of SPL has been studied, and is illustrated in Fig. 9(b). The output of the device was measured (using an Acoustic Calibrator), and found to be 0.03 pC/Pa. A flat frequency response has been obtained in the frequency range of 31–8000 Hz. This also supports the microtunnel design in this frequency range. The maximum sensitivity of the sensor

was found to be 382 μV/Pa. The average sensitivity of the ZnO thin film-based MEMS acoustic sensor is 382–191 μV/Pa.

V. Conclusion

A ZnO thin film-based MEMS acoustic sensor was successfully fabricated on SOI wafers having 25-μm-thick active layer using bulk-micromachining technique. The process was standardized for SOI wafers and diaphragm thickness uniformity of 25 μm $\pm$ 0.5 μm was observed. Bonding was performed before ZnO deposition to prevent the deterioration in ZnO film by high-temperature processing. ZnO etching by weak acid NH_4Cl with electrolytically-added copper ions improved the step coverage considerably and like in [20], no failure was observed under similar conditions. A smooth microtunnel without any blockage has been successfully fabricated for pressure compensation. The comparison of proposed technique with earlier technique [20] is given in Table III. The process has been significantly simplified providing better yield. Microtunnel blockage problem has been overcome by modifying the dicing parameters. A very high sensitivity of 382 μV/Pa has been achieved for 2.4 μm-thick ZnO film.

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