Accurate and efficient Estimation of Dynamic Virtual Ground Voltage in Power Gated Circuits

***Abstract*—Virtual ground voltage (V_{gnd}) is an important parameter that must be accurately and efficiently estimated during fine grained power gating of digital logic circuits. In this paper, We analyze the potential sources of error in dynamic characteristics of V_{gnd} due to inaccurate models and under-estimation of input voltages of CMOS gates in logic circuits. We propose a piecewise simulation based model for dynamic V_{gnd} estimation which further needs capacitance models to be characterized at V_{gnd} node. These capacitance models are used in conjunction with leakage current models to develop dynamic V_{gnd} model. Average error of less than 0.5% compared to 4.2% of previously developed models is achieved when compared to HSPICE results on ISCAS'85 benchmark circuits. On an average, our proposed model is 30× efficient than HSPICE for dynamic V_{gnd} estimation during mode transition.**

***Index Terms*—Power gating, Support Vector Machine (SVM), Leakage current, Transistor stacks, Virtual ground voltage, CMOS gates.**

I. Introduction

With the rapid scaling of MOSFET technologies, the contribution of leakage power to the total power is increasing. Power gating technique has been applied for reducing leakage power. Various issues such as - performance degradation, ground bounce noise, wake-up energy consumption, data retention, virtual ground or virtual supply voltage etc. need to be considered before applying it to the logic circuits. Power gating is coarse-grained generalization of MTCMOS technique in which high threshold transistor is inserted in pull-down and/or pull-up network as a footer in ground gating case Figure 1.(a) or header in supply gating case Figure 1.(b) or combined gating case. When the sleep transistor is in 'OFF' state during the standby mode of logic cluster, the leakage current flowing through logic cluster (I_{LC}) charges the V_{gnd} and reduces the effective supply to ground voltage across logic cluster and hence, reduces the leakage current across the gated circuit. In this paper, we explain our methodology considering ground gating case. However, the similar approach can be applied for the supply gating and combined gating case.

II. Previous Work on Virtual Ground Voltage Estimation and Motivation

In Recent years, V_{gnd} has been the basic parameter for development of many variants of power gating techniques. Singh *et. al.* [1] represents the leakage current of logic cluster and footer transistor as a function of V_{gnd}, then both currents are made equal to find the exponential linear model of V_{gnd} as a function of design parameters of logic cluster and footer transistor. The V_{gnd} calculated in [1] is a static voltage but it is a dynamic characteristic whose value is increased from lower to higher steady state value after the circuit is gated. Xu *et. al.* [2] estimates the dynamic virtual ground voltage during the mode transition which is further used to estimate energy consumed due to the transition of the V_{gnd} value, allowing the fine grained optimization of power gated circuits. Tovinakere *et. al.* [3] derive the semiempirical model for dynamic V_{gnd} estimation. Since, leakage will vary according to the design parameters of the footer transistor, so we need a quick exploration of design parameter space

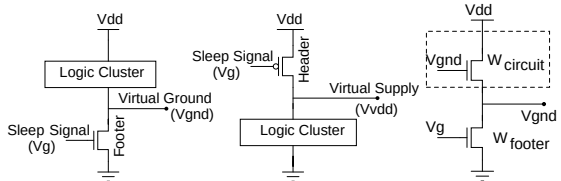


Figure 1. Power gating a) Ground gating case b) Supply gating case c) Equivalent circuit for V_{gnd}

for each input vector. Thus, there is clearly need of developing V_{gnd} model efficiently and model should also be highly accurate and fast. Next, we show the error incurred by previous models in terms of inaccurate leakage models for power gated circuits and assumption of inaccurate voltage conditions at the input of CMOS gates in power gated circuits.

A. Inaccuracy of previous models due to inaccurate leakage models

To calculate V_{gnd}, authors in [1], [2] represent the leakage current of logic cluster (I_{LC}) as an exponential linear function of virtual ground voltage which assumes the identical voltage at the input of the equivalent transistor and virtual ground node as shown in Figure 1.(c). Since, the exponential linear behavior of I_{LC} with respect to V_{gnd} is not valid rather it depends upon the type of circuits and their corresponding input vectors which may results in higher error for leakage modeling of logic cluster and consequently in static V_{gnd} estimation. From 1.(c), static V_{gnd} can be estimated by equalizing the leakage current of logic cluster and footer transistor using (1).

$$I_{LC}(logic-cluster) = I_{footer}(footer-transistor) \quad (1)$$

From [4], sub-threshold leakage current of a single 'OFF' transistor can be represented as in (2).

$$I = A.e^{1/mV_T(V_g - V_s - V_{th0} - \gamma^{'}V_s + \eta V_{ds})}.(1 - e^{-V_{ds}/V_T}) \quad (2)$$

$$\text{with } A = \mu_0 C_{ox}^{'} \frac{W}{L_{eff}} (V_T)^2 c^{1.8} c^{-\triangle V_{th}/\eta V_T}$$

Here, V_{th0} is the threshold voltage at zero body bias, V_T is the thermal voltage, $\gamma^{'}$ is body bias coefficient, η is the DIBL coefficient V_g, V_s and V_{ds} are gate, source and drain to source voltages respectively. In [1], [2], for $V_{ds} \gg V_T$, the term $(1-e^{-V_{ds}/V_T})$ in (2) is neglected. Authors in [1], represented (2) as a exponential linear function of V_{gnd}, logic cluster and footer transistor design parameters while in [2], it is denoted only in terms of V_{gnd} as shown in (3) and (4) respectively.

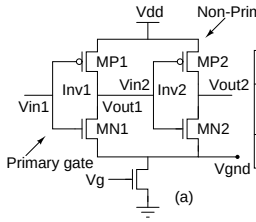
$$I_{leak} = I_0 \frac{W}{L} 10^{(-V_{th} - (\eta V_{gnd})/S_S)} \quad (3)$$

$$I_{leak} = \hat{I_N}.e^{-K_N V_{gnd}} \quad (4)$$

Neglecting the term $(1-e^{-V_{ds}/V_T})$ in (2) for higher values of V_{ds} i.e. low source voltage for fixed drain voltage (V_{dd} in case of logic cluster) causes error in estimating sub-threshold leakage current of a transistor for comparable values of V_{ds} and V_T. The authors in [3] represent leakage current as a polynomial function of degree N in terms of V_{gnd} as shown in (5).

$$I_{leak} = \sum_{j=0}^{N} p_j V_{gnd}^j \quad (5)$$

These types of model can result in very large error in estimation of the leakage current of logic cluster. There is a need for a kind of dynamic model without pre-assuming any kind of exponential or polynomial form and can capture relation of I_{LC} in terms of V_{gnd} more accurately. Authors in [5], evaluate the accuracy of previously reported leakage models using advanced BSIM4 transistor model [6]. State-of-the art methods use the leakage models in the exponential linear (EL) and 3^{rd} order polynomial (poly3) form as function of different parameters. The average error in mean and standard deviation of leakage can go upto ∼20% and ∼40% respectively. It has been observed that regression based non-linear modeling methods such as Neural Networks, Support Vector Machine are more accurate than exponential linear or polynomial models to establish the non-linear relationship between input and output parameters.



V_{gnd} (mV)	200	500	700	800	900
Vout1/Vin2 (mV)	200.01	500.01	700.63	808.61	980.87
Vout2 (mV)	999.98	999.99	999.99	999.95	992.64

(b)

Figure 2. Input voltages estimation for CMOS gates with non-primary inputs in ground gating case

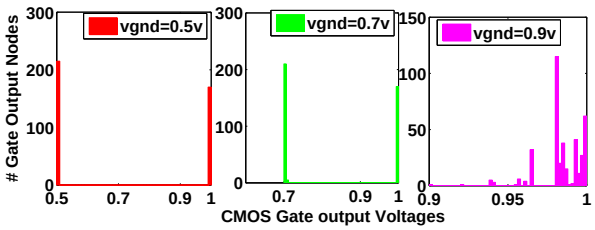


Figure 3. Fraction of number of CMOS gates presented in C880 ISCAS'85 benchmark circuit with output node voltages ranging between $0V$ to V_{dd} for varying V_{gnd}

B. Inaccuracy of previous models due to inaccurate assumption of input voltages of CMOS gates in power gated circuits.

Authors in [2], [3] model the logic circuit leakage during mode transition considering the effect of input states and circuit topologies. But these models do not consider the accurate input voltage conditions, which depends upon the V_{gnd}. They consider the input voltage at output of CMOS gates in the circuit as either V_{gnd} or V_{dd} for the whole virtual ground node voltage varying from $0\,V$ to V_{dd}. However, this is only true for the lower values of V_{gnd} in ground gating case. for higher values of V_{gnd}, both pull down network (PDN) and pull up network (PUN) are 'OFF', which makes the output voltage of that gate settle in between V_{dd} and V_{gnd}. This makes the input voltage of other gates different than the V_{gnd}. To explain it, first of all, we classify all CMOS gates in the circuit in two categories i.e. primary gates and non-primary gates. Primary gates are the CMOS gates of the circuit whose all inputs are supplied by users and inputs of non-primary gates are outputs of preceding gates. In Figure 2, 'Inv1' is the primary gate, which is receiving input from primary inputs whereas 'Inv2' is a non-primary gate whose input is a output of preceding gate 'Inv1'. Now suppose Vin1 = 1, MP1 is 'OFF' and thus 'ON'/'OFF' condition for MN1 and the input value at 'Inv2' gate will depend upon the value of V_{gnd}. **We define V_p as the maximum value of V_{gnd} for which pull down network is 'ON' for primary gate (In Figure 2, transistor MN1) and pull up network is 'ON' for non-primary gate (In Figure 2, transistor MP2).** This V_p defines the input voltage at non-primary gate 'Inv2'. For the lower values of V_{gnd} than V_p, NMOS transistor MN1 is 'ON' which makes the Vin2 same as V_{gnd}. For $V_{gnd} > V_p$, MN1 is 'OFF', i.e. Vin2 resides at the little bit higher value than V_{gnd} as follows.

$$Vin2 = \begin{cases} V_{gnd} & V_{gnd} < V_p \\ V_{gnd} + \triangle V & V_{gnd} \geq V_p \end{cases} \quad (6)$$

Here, $\triangle V$ is defined as the voltage drop across the pull-down network. Figure **2**.(b) shows the output/input gate voltage of primary/non-primary gate 'Inv1'/'Inv2' and output of 'Inv2' gate for the circuit given in Figure 2.(a). The difference between the V_{gnd} voltage and Vout1/Vin2 is very small for lower values of V_{gnd} because the pull down network (PDN) is 'ON' and drop across the PDN is very less and hence, can be removed from the circuit. Similarly, output of the non-primary gate 'Inv2' is close to the V_{dd} for lower V_{gnd} values and for higher values, this difference is high due to 'OFF' PUN network. For calculation of V_p, MN1 and MP2 transistors should be 'ON' simultaneously for input Vin1 = 1. Transistor MN1 will be 'ON' if gate to source (V_{gs}) is greater than threshold voltage of NMOS transistor (V_{thn}) i.e.

$$V_{gs}(MN1) > V_{thn} \quad (7)$$
$$V_{dd} - V_{gnd} > V_{thn} \quad (8)$$
$$V_{gnd} < V_{dd} - V_{thn} \quad (9)$$

Similarly, the condition for V_{gnd} to turn on MP2 can be described as.

$$V_{gnd} < V_{dd} + V_{thp} \quad (10)$$

From (9) and (10), V_p can be given as

$$V_p = min(V_{dd} - V_{thn}, V_{dd} + V_{thp}) \quad (11)$$

For Multiple input NAND type gates, if any input is connected to connected to logic '0', then output of that gate will be logic '1' irrespective of the V_{gnd} value. When all inputs are at logic '1', V_{gnd} will play an important role in deciding the output of a gate. On individual basis, maximum V_{gnd} for a gate depends upon the leakage i.e. input vectors of the gate. Leakage of a gate and V_{gnd} can be related as.

$$I_{LC} = I_{footer} \quad (12)$$

I_{footer}in terms of V_{gnd} can be given as[2].

$$I_{footer} = \begin{cases} \hat{I_f}.e^{K_N(V_{gnd}-V_{dd})} & V_{gnd} > 4V_T \\ 0 & V_{gnd} < 4V_T \end{cases} \quad (13)$$

From (12) and (13).

$$I_{LC} = \hat{I_f}.e^{K_N(V_{gnd}-V_{dd})} \quad (14)$$
$$V_{gnd} = V_{dd} + K_N^{'}.log(\frac{I_{LC}}{\hat{I_f}}) \quad (15)$$

From (15), V_{gnd} will be higher for high gate leakage. Generally leakage of a single gate is not enough to force the V_{gnd} to cross V_p. However in a circuit, maximum V_{gnd} for a gate will be decided by the leakage contribution of other CMOS gates also and can cross the V_p voltage. In a NAND type logic, PDN will be 'ON' if all transistors in a stack are 'ON'. Every transistor will have different V_{th} depending on it's location and terminal voltages in the stack. V_p will also be different for different gates. V_p for NAND type gates can be decided by the intersection of the V_p value of all NAND type gates as in (16). Similarly, V_p for NOR type gates can be described as in (17).

$$V_{p,NAND} = min(V_{p,INV}, V_{p,NAND2}, V_{P,NAND3}....) \quad (16)$$

$$V_{p,NOR} = min(V_{p,INV}, V_{p,NOR2}, V_{P,NOR3}....) \quad (17)$$

While computing V_p, PDN in NAND and PUN in NOR type gates must be 'ON' simultaneously. V_p of the complete circuit can be given by (16) and (17) as follows.

$$V_{p,circuit} = min(V_{P,NAND}, V_{P,NOR}) \quad (18)$$

The variation in V_{th} of different transistors in different CMOS gates makes the calculation of V_{gnd} a difficult exercise. For accurate computation of V_p, we slowly increase the V_{gnd} voltage and note the output node voltage of each gate in the circuit. However, V_p is one time calculation and will be same for all the circuit. Thus, HSPICE simulation can be used to compute V_p. By observing the node voltages in Figure **2**.(b), V_p can be given as $0.7\,V$. To check whether V_p voltage will be same for larger circuits, we simulate C880 ISCAS'85 benchmark circuit for different values of V_{gnd}. V_p value in this case is also $0.7\,V$. Here, we infer that if different circuits consist of CMOS gates from same logic library, then the V_p value will be same. One important observation to be made here is that the input gate voltages of the CMOS gates in any circuit can be predicted only for $V_{gnd} < V_p$. For $V_{gnd} > V_p$, leakage models for CMOS gates can not be used due to unknown input gate voltages. Compared to previous models, our methodology has the following advantages: 1) More accurate 2) Applicable to any circuit topology in static CMOS technology. 2) Includes effect on input states of CMOS gates. 3) Leakage models with all assumption removed.

III. Our Contribution

- We use SVM based regression models for leakage based on transistor stacks to remove the inaccurate assumption of EL and Poly3 model.

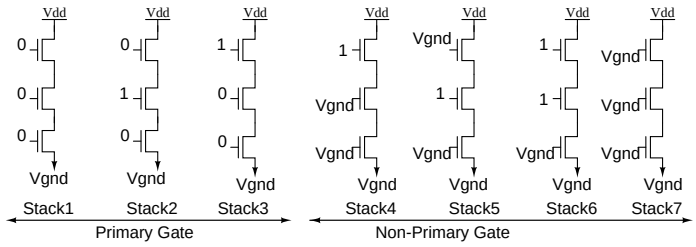


Figure 4. NMOS stacks with their possible terminal voltage conditions for primary and non-primary gates

- Our methodology uses the accurate value of leakage for primary or non-primary CMOS gates is for complete range of input varying from $0\,V < V_{gnd} < V_{dd}$.
- SVM based regression models are developed for capacitance estimation of CMOS gates at virtual ground node due to PDN network as a function of input voltage and V_{gnd} and for footer transistor as function of input voltage, width, V_{th} and V_{gnd}.
- Piecewise simulation based model is developed for dynamic V_{gnd} estimation which efficiently uses the pre-developed leakage and static V_{gnd} models along with extra capacitance models..

In Section IV, transistor stacks are characterized using regression based SVM models for leakage estimation of CMOS gates and elaborates our equivalent stack identification method based on the input gate voltages and V_{gnd}. Dynamic V_{gnd} estimation methodology is provided in Section 8. Experimental results are shown in Section VI. Finally we conclude in Section VII.

IV. SVM BASED LEAKAGE MODELING AND EQUIVALENT STACK MODELS EXTRACTION

In power gating case, the inputs of a primary and non-primary CMOS gates can take any value out of 3 values i.e. $0\,V$, $1\,V$ and V_{gnd}, some of the cases are shown in Figure 4. We formulate some rules for finding the equivalent stack model of a CMOS gate on the basis of type of the gate whether it is a primary or non-primary gate and the input to the gate because the input vectors have the significant impact on the leakage current of a CMOS gate. Consider a 2-input NAND gate as shown in Figure 5, with different input voltage conditions of primary and non-primary gates. In our methodology, we remove either PDN or PUN based on the input voltages and V_{gnd} value. These rules can be described as follows (The following rules are only for AND family of gates, similarly , rules can be described for OR family of gates):

1) For any primary gate, if any input to the CMOS gate is at logic '0', then remove PUN from that CMOS gate and connect output node to the V_{dd} because logic '0' input will make the PUN 'ON'. This rule is independent from the value of V_{gnd} because it does not affect the gate to source voltage of PMOS transistors in PUN.
2) For any primary gate, if all inputs are at logic '1' and if V_{gnd} is less than V_p, remove PDN and connect output node to V_{gnd} otherwise don't remove PUN and PDN.
3) For any non-primary gate whose all inputs are outputs of preceding gates, remove PUN if and only if $V_{gnd} < V_p$ because PMOS transistor in PUN makes the it 'ON' and output node can be connected to V_{dd} otherwise don't remove PUN and PDN.

Above rules can also be applied to parallel 'OFF' transistor stacks whether there is only one 'OFF' transistor in each stack or multiple 'OFF' transistors with 'ON' transistors in a stack. Equivalent model can be derived by summing the currents from all the stacks.

In this work, we assume that the maximum stack-size is 4 due to increased logical effort for higher order stacks. We have used conventions for labeling transistor stacks as: {stack type}{stack size}. Where, stack type indicates whether it is an NMOS stack or a PMOS stack. Stack size represents the number of transistors on a stack.

A flowchart to extract stack for AND family of gates is shown in Figure **??**. Extraction of stacks for 2-input NAND gate is shown in Figure 5. In our methodology, we remove either pull-down network (PDN) or pull-up network (PUN) based on the input voltages and V_{gnd} value. Figure 6 shows characterized transistor stacks for AND family of CMOS gates. Similarly, transistor stacks for OR family of gates can also be derived. We model a transistor stack of each size of NMOS and PMOS type. Models n1 to n4 are for CMOS gates in logic cluster whereas n1,f is for footer transistor which is different than model n1 with respect to the parameters used in the modeling. The final function that relates input and output using SVM can be described as:

$$y_k = \sum_{k=1}^{N} \alpha_k K(x_k, x) + b \tag{19}$$

Here $K(x_k, x)$ is the kernel function and α_k and b are solution of the linear systems [7].

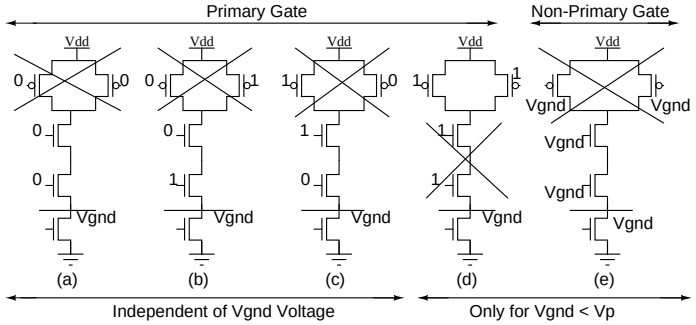


Figure 5. Equivalent stack models for NAND2 gate in ground gating case

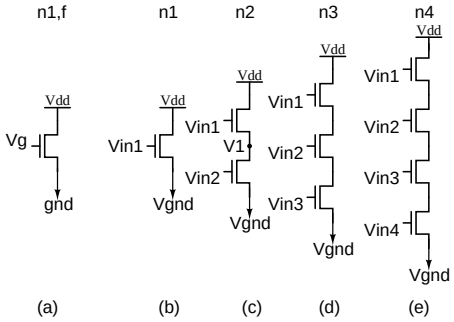


Figure 6. Characterized NMOS stack models in ground gating case

V. DYNAMIC V_{gnd} ESTIMATION

To apply power gating at circuit level, several configurations have been proposed trading-off between parameters such as - area, performance, maximum switching current. Distributed footer transistor based approach (DSTN) has been reported [8] which is compatible with timing-driven placement as well as reduces area for both footer transistors and wires. DSTN method is selected to verify circuit level V_{gnd} model. Figure 7 shows the circuit level DSTN methodology, consisting n number of clusters with n footer transistors. Each footer can be modeled with one current source $I_{footer,n}$. All footer transistors can be modeled as a single current source I_{footer}.

Figure 8 shows the typical characteristics of ground gated circuit during mode transition. In this section, we describe that how effectively our leakage models in Section IV can be used for dynamic V_{gnd} estimation. To model dynamic V_{gnd}, equivalent capacitance (C_{eq}) need to be considered at virtual ground node. C_{eq} can be calculated by summing the capacitances due to logic cluster (C_{LC}) and footer transistor (C_{footer}). The charging current across C_{eq} can be given as in (20).

$$I_{C_{eq}} = C_{eq}\frac{d_{V_{gnd}}}{dt} = I_{LC} - I_{footer} \tag{20}$$

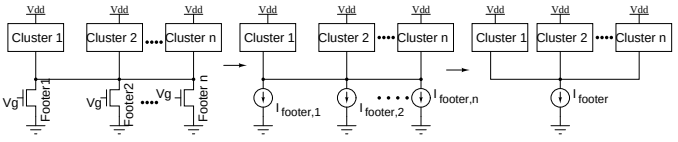


Figure 7. Circuit level DSTN method for Static V_{gnd} estimation

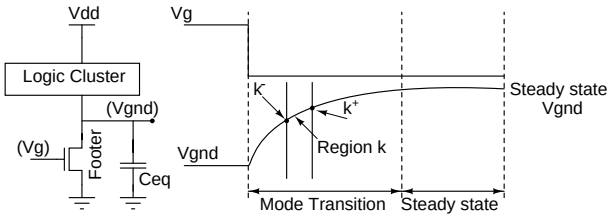


Figure 8. Dynamic V_{gnd} in ground gated circuits

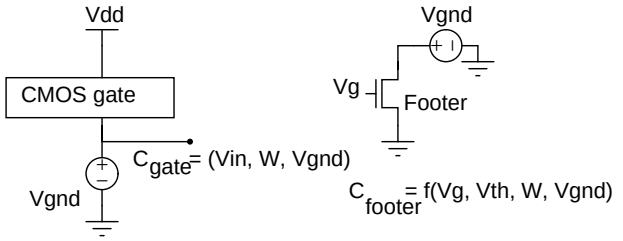


Figure 9. Models for capacitance estimation at virtual ground node

Here, I_{LC} and $I_{footter}$ are the leakage currents across logic cluster and footer transistor. To calculate V_{gnd} as in (20), C_{eq}, I_{LC} and $I_{footter}$ must be modeled in terms of V_{gnd}. I_{LC} and $I_{footter}$ models can be directly imported from the section IV but capacitance models are need to be developed. Since, capacitances at output nodes of CMOS gates affect the virtual ground node capacitance, hence we can not remove either PDN or PUN andC_{eq} is modeled using two types of model i.e. one for CMOS gates and other for footer transistor as shown in Figure 9. CMOS gate capacitance C_{gate} at virtual ground node is function of input voltages and V_{gnd}; while C_{footer} is modeled as function of footer transistor parameters (V_g, V_{thf}, W_{footer}) and V_{gnd}. Total number of N+1 models are required. Here, N represents the type of basic CMOS gates such as NAND2 NAND3, NOR2, NOR3 etc. (Ref. Table II) and one more model is required for footer transistor. Virtual ground capacitance for other gates is calculated using basic CMOS gate capacitances. SVM based regression models are used for capacitance models. Generally, capacitance at any node is assumed as linear function of gate to source voltage (V_{gs}) [9] but it is not always true. In fact, C_{gate} model will be non-linear function of input voltages and V_{gnd} and C_{footer} will be non-linear function in terms of footer transistor parameters. Since, SVM models are black-box models, the only limitation is that we do not know the equations for C_{eq}, I_{LC} and $I_{footter}$ in terms of V_{gnd}. Hence we propose piecewise simulation based model for dynamic V_{gnd} estimation. We describe our methodology in the following steps.

Step (1) - V_{gnd} is divided from $0\,V$ to V_p into k regions. k determines the trade-off between the runtime and accuracy of the model.

Step (2) - Capacitance C_{eq}^{k} is computed at virtual ground node for a given input vector (i) with N CMOS gates in logic cluster and M footer transistors (Consider DSTN method) at lower (k^-) and higher (k^+) value of region k as shown in Figure 8.

$$C_{eq}^{k} = C_{LC}^{k} + C_{footer}^{k} \tag{21}$$

Here,

$$C_{LC}^{k} = C_{gate,1}^{k} + C_{gate,2}^{k} + \ldots\ldots\ldots + C_{gate,N}^{k} \tag{22}$$

$$C_{footer}^{k} = C_{footer,1}^{k} + C_{footer,2}^{k} + \ldots\ldots\ldots + C_{footer,M}^{k} \tag{23}$$

Average $C_{eq}^{k,avg}$ is calculated as in (24).

$$C_{eq}^{k,avg} = (C_{eq}^{k^-} + C_{eq}^{k^+})/2 \tag{24}$$

Step (3) - Average charging current, $I_{C_{eq}}^{k,avg}$ is computed using (25).

$$I_{C_{eq}}^{k,avg} = I_{LC}^{k,avg} - I_{footer}^{k,avg} \tag{25}$$

Here,

$$I_{LC}^{k} = I_{gate,1}^{k} + I_{gate,2}^{k} + \ldots\ldots\ldots + I_{gate,N}^{k} \tag{26}$$

$$I_{LC}^{k,avg} = (I_{LC}^{k^-} + I_{LC}^{k^+})/2 \tag{27}$$

$$I_{footer}^{k} = I_{footer,1}^{k} + I_{footer,2}^{k} + \ldots\ldots\ldots + I_{footer,M}^{k} \tag{28}$$

$$I_{footer}^{k,avg} = (I_{footer}^{k^-} + I_{footer}^{k^+})/2 \tag{29}$$

Step (4) - In each region k, we consider a constant leakage across logic cluster and footer transistor. From (20), average charging current in region k can be given as follows.

$$I_{C_{eq}}^{k,avg} = C_{eq}^{k,avg}\frac{dV_{gnd}}{dt} = I_{LC}^{k,avg} - I_{footer}^{k,avg} \tag{30}$$

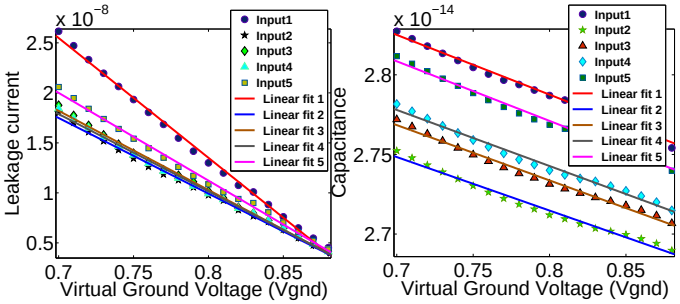


Figure 10. Leakage current and capacitance at virtual ground node during $V_p < V_{gnd} < V_{steady,state}$ for different input vector combinations of C880 ISCAS'85 benchmark circuit

$$\frac{V_{gnd}^{k^+} - V_{gnd}^{k^-}}{T^{k^+} - T^{k^-}} = \frac{I_{LC}^{k,avg} - I_{footer}^{k,avg}}{C_{eq}^{k,avg}} \tag{31}$$

$$T^{k^+} - T^{k^-} = (V_{gnd}^{k^+} - V_{gnd}^{k^-}) * \frac{C_{eq}^{k,avg}}{I_{LC}^{k,avg} - I_{footer}^{k,avg}} = \alpha \tag{32}$$

$$T^{k^+} = T^{k^-} + \alpha \tag{33}$$

Equation (33) provides the estimate of time duration that circuit takes in charging virtual ground node from $V_{gnd}^{k^-}$ to $V_{gnd}^{k^+}$. T^{k^-} for first region will be 0 sec. T^{k^+} of each region will be T^{k^-} for the region $k+1$.

Step (5) - In step (1), V_{gnd} range is partitioned from $0\,V$ to V_p only because inputs of CMOS gates in the circuit are not known and hence, we are unable to find capacitances and currents during $V_{gnd} > V_p$. At $V_{gnd} = V_p$, capacitance and currents at virtual ground node are known. Now, we define a steady state virtual ground voltage ($V_{steady,state}$) which is the maximum value of virtual ground node. Current across C_{eq} will be zero and current across logic cluster will be same as footer transistor.. $V_{steady,state}$ is calculated by SPICE simulation and it is one time calculation for a circuit. From Figure 10, it can be inferred that the current and the capacitance of logic cluster is linear for $V_p < V_{gnd} < V_{steady,state}$. Using two points, V_p and $V_{steady,state}$, linear equation is obtained in MATLAB curve fitting toolbox. Correlation coefficient (ρ) of greater than 0.995 is obtained with linear fitting. This linear equation can now be used in V_{gnd} estimation for remaining range of V_{gnd} and steps (1) to (4) are repeated until $V_{steady,state}$ is reached.

Our approach for dynamic V_{gnd} estimation is more accurate than [2] due to use of accurate leakage and capacitance models for $V_{gnd} < V_p$ without any assumption and without neglecting any term in the device model equations. Linear form of logic cluster current and capacitance is assumed Only for $V_p < V_{gnd} < V_{steady,state}$ which is also highly accurate assumption. In [2], a piecewise exponential linear model is developed in which complete range is divided into regions and linear equations for logic cluster current and footer transistor are obtained through fitting in these regions. These fitted equations are used in (20) to find out the resulting expressions for V_{gnd} the considered region. Capacitance variation in the partitioned region is considered as constant which incurs high error in models [2]. While, in our proposed model, we divide it sufficiently large number of regions such that capacitance can be treated as a constant in each region. Multiple fitting points in each region are considered separately which results into more accurate capacitance in complete range of V_{gnd}. Another important limitation and source of error of model in [2] is the unknown input voltages of CMOS gates for $V_p < V_{gnd} < V_{steady,state}$ and hence, linear current equations and capacitances can not be evaluated. Our proposed model mitigates this error situation

VI. Experimental Results

We have used LS-SVM toolbox which is an advanced version of SVM for improving efficiency of the model. Radial Basis Function (RBF) kernel $K(x, x_k) = exp(||x - x_k||^2/\sigma^2)$ is used in models. Model for V_{gnd} model is developed in terms of width (W_{footer}), input voltage (V_g) and threshold voltage (V_{th}) of the footer transistor within ranges of $28nm$ - $500nm$, $0\,V$ - $0.25\,V$, $0.4\,V$ - $0.6\,V$ respectively.

Table I
MEAN SQUARE ERROR AND CORRELATION COEFFICIENT OF TRAINED NMOS STACKS

Model	# Training Samples	T_{model} (s)	MSE	ρ	T_{run} (μs)
n4	1000	147.89	1.14e-12	0.9995	254.5
n3	850	120.45	2.07e-13	0.9995	216.4
n2	700	112.33	1.56e-13	0.9996	179.0
n1	550	82.78	9.42e-14	0.9998	141.8
n1,f	600	88.40	1.01e-13	0.9996	154.3

$T_{model} \rightarrow$ Model Characterization time, $\rho \rightarrow$ Correlation coefficient, *MSE* $\rightarrow$ Mean Square Error, $T_{run} \rightarrow$ Model Runtime

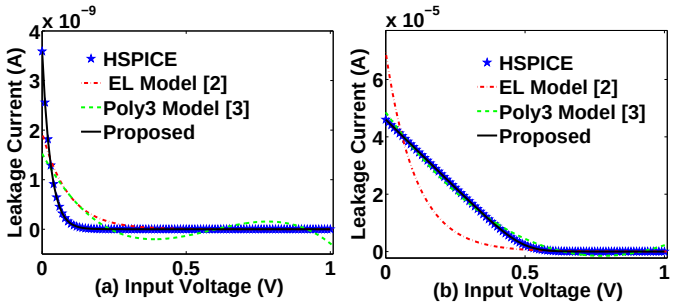


Figure 11. Leakage model comparison for n1 stack in Figure 6.(a) for different values of input voltage (Vin1) and V_{gnd}. (a) $V_{gnd} = 0\,V$ (b) $V_{gnd} = 1\,V$

A. Evaluation of Leakage Current Estimation models

In this section, we describe the results for evaluation of accuracy and efficiency of proposed leakage current models. Table I shows that efficiency of proposed sample selection method which require less samples than previous techniques. We use 5000 test samples to evaluate the accuracy of the models. Near one correlation coefficient and lower MSE shows high accuracy of our characterized stack models with respect to HSPICE output.Proposed models training time is higher for higher order stacks, however simulation time is almost same for all stack models which indicates that it is less dependent on the order of stack models. In Table I, we do not include the information related to PMOS stack models. In case of PMOS stacks, training time and simulation time is approximately same because time factor does not depend upon the type of models instead it depends only on number of training samples. MSE and correlation coefficient are also of the same order as NMOS stacks. Figure 11 shows the curve fitting of the EL model [2] and poly3 model [3] for n1 stack model in Figure 6.(b). We infer from our experiment that the neither EL model nor poly3 model is able to fit the HSPICE data accurately for V_{gnd} voltage varying from $0\,V$ to $V_{dd}$and the use of SVM models with better accuracy than EL and poly3 models is justified.

Figure 12 shows C17 circuit from ISCAS'85 benchmarks and it's corresponding stack models for input vector '00000'. Equivalent stack models are developed based on the rules as described in Section IV, which are only valid for $V_{gnd} < V_p$; hence, we compare our results in this range only. Figure 13 shows the comparison of leakage current of the C17 circuit for different V_{gnd} values using EL, Poly3 and proposed model. It can be concluded that proposed model accurately tracks the HSPICE output compared to the large error of EL and Poly3 model.

B. Evaluation of Circuit level Dynamic V_{gnd} model

According to proposed piecewise simulation based methodology for dynamic V_{gnd} estimation , capacitance models are required with leakage models. The virtual ground capacitance is modeled for each gate type and footer transistor. The number of capacitance models to be characterized, depends upon the number of gates from the cell

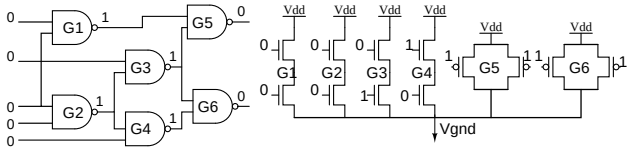


Figure 12. C17 circuit diagram and it's equivalent stack model representation for input '00000'

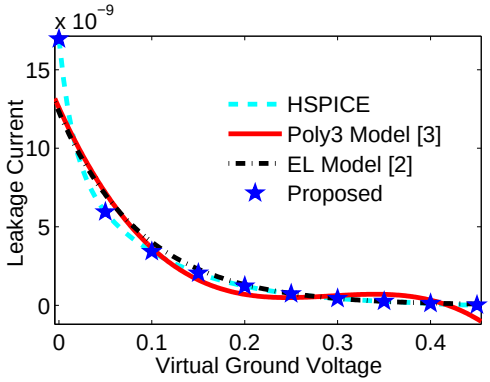


Figure 13. Comparison of leakage current estimation models using [2], [3] and our method for C17 circuit with input vector '00000'

Table II
ERROR OF CAPACITANCE MODELS FOR BASIC CMOS GATES

Gate	T_{model} (s)	Training Samples	MSE ($\times 10^{-4}$)	Correlation Coefficient	% Error Max	% Error Avg	T_{run} (μs)
NAND2	110.45	850	3.11	0.9968	1.05	0.109	189.6
NAND3	130.68	950	3.45	0.9968	1.16	0.314	197.6
NAND4	155.56	1000	4.22	0.9961	1.20	0.368	201.7
NOR2	129.89	950	3.23	0.9969	1.05	0.239	189.7
NOR3	126.78	950	5.14	0.9960	1.26	0.365	198.0
NOR4	159.98	1050	5.20	0.9961	1.29	0.430	203.8
INV	102.23	600	3.04	0.9970	1.02	0.106	184.5

library used for synthesizing the logic circuit. Table II shows the error in capacitance modeling for basic CMOS gates of a standard cell library. We consider a CMOS gate with maximum 4 inputs, as higher input gate will have the large delay due to increased logical effort. Adaptive sampling method described in Section **??** is used to reduce the number of training samples. Error for OR family of gates is little bit higher than AND family of gates because of directly connecting the higher number of transistors to the V_{gnd} node. However, capacitance model for each gate has less than 1% average error and maximum error is also between 1% to 2%. Low MSE and high correlation coefficient confirm the high accuracy of proposed capacitance models.

As shown in Figure 14, capacitance estimation for NAND2 gate virtual ground node from proposed model lie on the curve obtained using HSPICE and hence, confirm the higher accuracy of proposed capacitance model. For higher V_{gnd} and increasing values of input voltage, change in the capacitance is very less and almost a linear curve is obtained. however, lower values of V_{gnd} introduce non-linearity for the same input voltage range. Proposed SVM models are able to handle this non-linearity with high accuracy.

Dynamic V_{gnd} model is verified using circuits from ISCAS'85 benchmark circuits. We consider 100 input vectors for each circuit and for every input vector, V_{gnd} voltage range from $0\,V$ to V_p is divided into 90 regions and 10 regions are chosen for $V_p < V_{gnd} < V_{steady,state}$. for any circuit, if $V_{steady,state} < V_p$ then all 100 points are selected within $0\,V < V_{gnd} < V_p$. We compare our model with the piecewise linear model in [2], where authors divided V_{gnd} voltage range from $0\,V$ to V_{dd} in 18 regions. Runtime of proposed SVM model is estimated as in (34).

$$T_{ours} = [T_{I,LC} + T_{cap,LC}]_{SVM,90} + T_{fit-cap,LC,1} + \ldots + T_{fit-I,LC,1} + [T_{I,LC} + T_{cap,LC}]_{fit,10} + \ldots + [T_{I,footer} + T_{cap,footer}]_{SVM,100} + T_{dyn-vgnd,100} \quad (34)$$

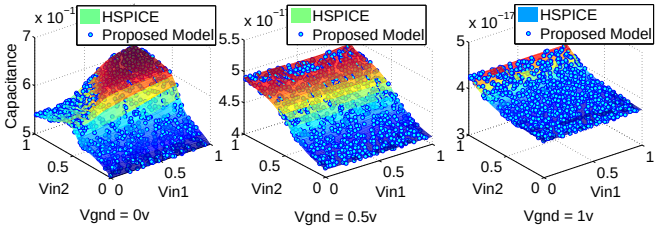


Figure 14. Capacitance variation at virtual ground node of NAND2 gate for different V_{gnd}

Table III
DYNAMIC V_{gnd} MODEL RESULTS FOR ISCAS'85 BENCHMARK CIRCUITS

Circuit	Error (%)				Runtime (sec.)			Speedup(×)	
	Maximum		Average		HSPICE	[2]	Proposed	[2]	Proposed
	[2]	Proposed	[2]	Proposed					
C17	7.62	0.67	3.66	0.12	12.66	1.08	1.46	12	8
C432	6.64	0.68	5.10	0.11	60.45	1.62	2.56	37	23
C499	7.40	0.79	4.12	0.15	117.89	3.49	5.22	33	22
C880	5.30	1.02	3.66	0.56	72.70	2.73	4.02	26	18
C1355	8.33	1.10	4.83	0.49	110.23	2.90	5.11	38	21
C1908	6.42	0.98	4.95	0.72	136.56	3.89	5.29	35	25
C2670	7.93	0.75	4.36	0.67	143.78	3.45	5.48	41	26
C3540	5.31	1.17	3.22	0.88	162.33	4.32	4.92	37	33
C5315	6.88	1.16	4.37	0.80	201.34	4.11	6.24	49	32
C6288	5.66	0.92	2.92	0.13	228.30	2.01	2.23	113	102
C7552	9.41	1.20	4.99	0.83	300.69	4.65	6.93	64	43
Overall	6.99	0.95	4.20	0.45	140.63	3.11	4.50	45	31

Table IV
% ERROR IN ENERGY CONSUMED ESTIMATION DURING MODE TRANSITION FOR ISCAS'85 BENCHMARK CIRCUIT

Circuit	Error (%)			
	Maximum		Average	
	[2]	Proposed	[2]	Proposed
C17	11.60	1.69	7.65	1.31
C432	9.78	1.68	6.11	1.12
C499	10.46	1.78	6.10	1.15
C880	10.45	2.19	7.54	1.55
C1355	11.01	2.16	6.80	1.50
C1908	8.40	1.79	5.95	0.89
C2670	10.89	1.79	7.34	1.71
C3540	9.10	1.11	6.20	0.98
C5315	10.81	1.16	5.45	1.10
C6288	7.12	0.99	4.21	0.79
C7552	12.48	2.45	7.90	1.96
Overall	10.19	1.71	6.48	1.28

Here, $[T_{I,LC} + T_{cap,LC}]_{SVM,90}$ denotes the total runtime of logic cluster for leakage current estimation ($T_{I,LC}$) and capacitance calculation ($T_{cap,LC}$). Runtime is estimated by simulating SVM models 90 times during $0V < V_{gnd} < V_p$. $T_{fit-cap,LC}$ and $T_{fit-I,LC}$ determine the runtime to fit the linear model for capacitance and leakage current estimation of logic cluster during $V_p < V_{gnd} < V_{steady,state}$. Only one time fitting is required for each one of two models. $[T_{I,LC} + T_{cap,LC}]_{fit,10}$ indicates the runtime of the fitted models in $T_{fit-cap,LC}$ and $T_{fit-I,LC}$ and these models are simulated for 10 times. Next, the $[T_{I,footer}+T_{cap,footer}]_{SVM,100}$ evaluates the runtime of leakage and capacitance models for footer transistor and for all 100 regions, SVM models are used. $T_{dyn-vgnd,100}$ calculates the runtime of the (33) for each region. Runtime of the model in [2] can be given as follows.

$$T_{[4]} = [T_{fit-I,LC} + T_{I,LC} + T_{fit-I,footer} + T_{cap,LC} + ... \\ ... + T_{I,footer} + T_{cap,footer} + T_{dyn-vgnd}]_{18} \quad (35)$$

Each term in (35) is evaluated 18 time i.e. one time for each region. It should be noted that linear fitting models are used only for leakage current of logic cluster and footer transistor. In each region, capacitance is considered to be a constant value. The maximum and average error with average runtime across all input patters is shown in Table III. Proposed model incurs an order less error than model in [2]. Figure 15 shows the dynamic V_{gnd} characteristics of C880 ISCAS'85 benchmark circuit after the sleep mode is ON. Proposed model almost tracks HSPICE simulation, whereas previously reported model incurs ~ 10 % error. We have implemented the consumed energy estimation methodology in [2] during mode transition for a dynamic V_{gnd} characteristics of benchmark circuits. Percentage error in energy estimation is given in Table IV. Less error in energy estimation shows the higher accuracy of our proposed of dynamic V_{gnd} estimation.

However, proposed model is 30× times faster than HSPICE but a bit slower than model in [2]. This is because of the large number of points taken in range from $0V$ to V_{dd}. Runtime of our models can be further reduced by taking less number of simulation points between $0V$ and $V_{steady,state}$. Figure 16 plots the accuracy - runtime trade-off with respect to the number of simulation points for C7552 ISCAS'85 benchmark circuit. From Table III, number of simulation points for proposed dynamic V_{gnd} models should be less than 43 to make runtime less than in [2]. At this number, the error incurred is ∼1.8% which is less than 4.99% of the model proposed in [2].

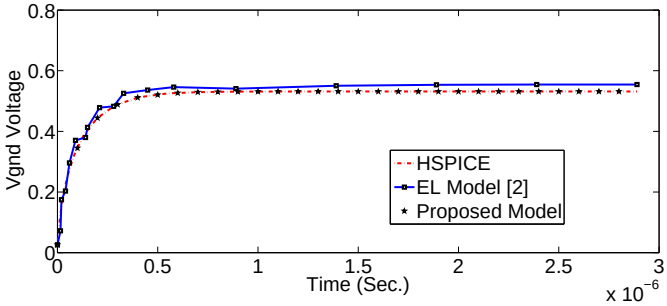


Figure 15. Dynamic V_{gnd} voltage during model transition for C880 circuit

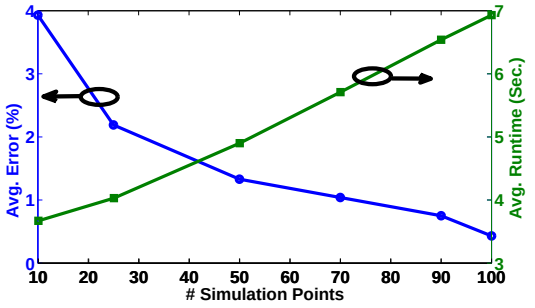


Figure 16. Effect of number of simulation points on accuracy and runtime of dynamic V_{gnd} model

VII. CONCLUSION

In this manuscript, we have proposed and proved the efficacy of novel approach for estimation of dynamic V_{gnd}, which can further be utilized energy consumption during mode transition from active to sleep state. SVM based regression models are proven to be more accurate than earlier proposed analytical models. Piecewise simulation based dynamic V_{gnd} estimation methodology is developed, which uses models for leakage current as well as capacitance at virtual ground node. Our proposed dynamic V_{gnd} models are very close to the HSPICE results with average error of less < 1% on ISCAS'85 benchmark circuits whereas speedup of 30× is achieved compared to HSPICE.

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