Variation Robust Subthreshold SRAM Design with Ultra Low Power Consumption

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Abstract. Continued scaling of CMOS technologies has resulted in process variations emerging as a critical design concern. The power consumption requirement in portable devices is even more strictly constrained for extending the battery operating lifetime. In this work, we propose an asymmetrical Schmitt trigger based SRAM cell, suitable for ultra low power applications. It addresses the fundamental conflicting design requirement of read versus write operation of conventional 6T cell. A built-in feedback mechanism proposed for the cell, makes it more robust against process variations. Usually, a Schmitt trigger cell configuration has been used in literature for improving stability of inverter-pair. We propose asymmetrical cell-configuration as modification over this usual Schmitt-trigger based configuration so that the design becomes more tolerant of mismatch in neighboring transistors. Simulation results show that proposed bitcell operates on a very low leakage current and with much less power dissipation compared to 6T cell.

Keywords: Low voltage/Subthreshold SRAM Design, Low power SRAM, Process variation, Schmitt trigger.

1 Introduction

It is expected that more than 90% of the die area in future systems-on-chip (SoCs) will be occupied by SRAM and the requirements of higher density and low power SRAMs are increasing exponentially. The main sources of power consumption in digital Complementary Metal Oxide Semiconductors (CMOS) circuits are logic transitions, short circuit currents that flow directly from supply to ground when both n and p sub network conducts simultaneously and leakage current that accounts for static power dissipation. The active power dissipation in the switching parts of the circuit increases with improved performance and increased density with each technology generation. Leakage mainly consists of gate leakage and subthreshold leakage. The magnitude of leakage current is no longer negligible and it plays a significant role in total power consumption at lower technology nodes. For portable devices developed for 65nm technology node, it is estimated that subthreshold leakage power will account for about 50 percent of the total power consumption [1]. Ultra low power design is always on demand as it can meet the requirement of

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extending battery life of portable electronic devices like smart phones, digital cameras, biomedical chips etc.

Different power reduction techniques like voltage scaling, pipelining, device & interconnect sizing and switching activity reduction have been implemented at device/circuit/architectural level. Among these, supply voltage scaling has remained one of the first choice of designers. The dynamic power can be reduced quadratically and leakage power linearly to first order by reducing supply voltage [2].

In a given process technology, the process constraints such as gate oxide limits the maximum supply voltage (V_{max}) for transistor operation and for a given performance requirement, the minimum supply voltage (V_{min}) is limited by increased process variation and sensitivity. With technology scaling, the V_{max} increases while the V_{min} increases. Therefore for low power operation, the V_{min} has to be lowered further to increase the SRAM bitcell operation range.

1.1 Process Variation

The major roadblock that designers face is process variation, as high performance processors move to sub 45nm technologies. The process parameter variation results in variation in maximum operating frequency and power consumption in fabricated dies [3]. Process variation can be due to variation in parameter, voltage and temperature. Inability to precisely control the fabrication process at nanometre technologies, results into parameter variation. Parameter variations can be mainly classified in to two categories- (i) Die to Die (D2D) variations, which affects all the transistors in a lot or wafer equally and (ii) With-in die (WID) variations, consisting of systematic and random components, causes electrical characteristics to vary across a die [4]. For a given design, both, power supply and temperature vary from chip to chip and within chip. Voltage variation can be caused by IR drops in the supply networks or by LdI/dt noise under changing load. Spatially and temporally varying factor causes temperature variations. All these variations cannot be tolerated as technology scales to smaller feature sizes.

In ultra low power designs, the sensitivity of circuit parameters increases with reduction in supply voltage. Memory cells are most sensitive to device variations causing device mismatch for several reasons. Therefore the process variation limit the circuit operation in sub threshold region, particularly in SRAM cells where minimum sized transistors are used. For several reasons memory cells are most sensitive to device variation which results in device mismatch. Usually the devices used in smallest memory cell for a given process, is smaller than the devices allowed elsewhere in the design [5].

1.2 Earlier Work on Process Variation Tolerant SRAM Bitcell

The 6 transistor (6T) cell which uses a cross-coupled inverter is the basic memory bitcell used in SRAM designs. Several SRAM bitcells have been proposed to meet different design goals such bitcell area, low voltage/ low power operation, timing specifications, bit density and reliability. To improve process variation tolerance,

adaptive circuit techniques like source biasing and dynamic VDD have been proposed [6]. Different types of Single ended and differential operating bitcells have been proposed. For achieving improved read stability, different bitcell configurations use an extra sensing circuit for reading cell contents. Considering the fact that the stability of the inverter pair should be improved for stable SRAM operation at low supply voltages, Jaydeep P. Kulkarni et. al had proposed a Schmitt trigger based differential bitcell having built-in feedback mechanism for improved process variation tolerance [7].

The rest of this paper is organised as follows. In Section 2 the operation of basic SRAM cell, conflicting read vs. write design requirement and Schmitt trigger principle for cross-coupled inverter pair are discussed. Section 3 describes proposed SRAM bitcell. Section 4 covers the simulation results and paper concludes with Section 5.

2 Conventional 6T SRAM Bitcell

The basic static RAM cell is shown in Fig. 1. It consists of two cross-coupled inverters and two access transistors. Four of the transistors are used to make a pair of inverters – NOT gates, essentially. Each inverter requires a pair of transistors – if the input is 0, then the p-type transistor will be on, and the n-type off. This will connect the output to power, which is equal to logic 1. Otherwise, if the input is 1, the output will be connected to ground, or logic 0.

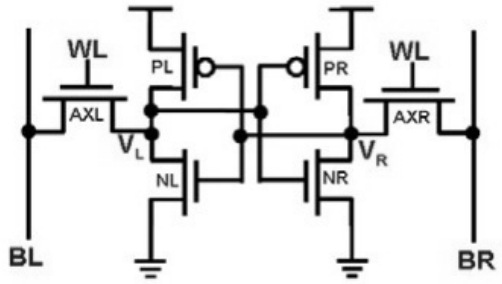

Fig. 1. Conventional symmetrical 6T bitcell

The two inverters are connected in a loop, with the output of one, the input of the other. The access transistors are connected to the wordline at their respective gate terminals, and the bitlines at their source/drain terminals. The wordline is used to select the cell while the bitlines are used to perform read or write operations on the cell. Internally, the cell holds the stored value on one side and its complement on the other side.

This arrangement has two stable states: we interpret these two states can be interpreted as 1 and 0. The other two transistors are used to control reading and writing. To read the contents of the RAM cell, the *word* line (WL) is set high,

allowing the contents of the cell to be read out to the *bit* line say BL (and its inverse) to the *not bit* (BR) line. To write the cell, we again set the *word* line high, but this time we set the *bit* line (and its inverse) to the value we wish to store, forcing the cell into the appropriate state.

2.1 Conflicting Read vs. Write Design Requirement in 6T bitcell

For reliable read operation, the design requirement is such that the data should not be flipped. However during the write operation, the design requirement is such that the data should be flipped as easily as possible. This is the fundamental conflicting design requirement in the conventional 6T bitcell. This is because; the same pair of access transistors is used to initiate read/write operation in a 6T cell. Traditionally device sizing has been adopted to balance the read versus write design requirements. With increased process variations, satisfying the conflicting requirements during read-write operation is becoming very challenging [8]. This degrades the scalability of the SRAM cell as well. Moreover, device sizing is not effective for improving the cell stability at very low supply voltage [9]. Hence there arises a need for a novel design approach for successful low voltage operation of SRAM bitcells in nano-scaled technologies.

In order to resolve the read versus write conundrum in the 6T cell, Schmitt trigger principle for the cross coupled inverter pair had been proposed [10]. A Schmitt trigger is used to modulate the switching threshold of an inverter depending on the direction of the input transition.

3 Proposed Asymmetric SRAM Bitcell

Fig. 2 shows the schematics of proposed asymmetrical Schmitt trigger based bitcell. For maintaining the clarity of discussion, the bitcell configuration in [10] is termed as ST bitcell while the bitcell we proposed is termed as AST bitcell hereafter in this paper. The AST bitcell have 10 transistors, 2 wordlines (WLL /WLR) and 2 bit-lines (BL/BR). Transistors PL-NL1-NL2-NFL form ST- I inverter while PR-NR1-NR2-NFR form ST- II inverter. Feedback transistors NFL/NFR raise the switching threshold of the inverter during the 0→1 input transition giving the Schmitt trigger action.

Asymmetric cell (AST) differs from usual 6T and Schmitt trigger based SRAM cell in following manner.

- Read bitline (RBL) is separate from write bitline (WBL). This means that the read operation is performed independent of the right side bitline, unlike the traditional 6T/ ST cell which uses both bitlines simultaneously for read access and write operation.

- Read wordline (RWL) is separate from write wordline (WWL).This means that for read access the new cell only asserts RWL to enable the left switch pass transistor and the right pass transistor is kept off. This is opposite to conventional 6T/ST cell which uses both pass transistors by asserting common WL for read or write operation. Hence, the read access is performed only through the left side of the cell using RBL precharged high and then asserting the RWL. On the other hand, the write operation is accomplished only through the right side of the cell by enforcing the WBL to the desired value and then asserting the WWL, independent of the left side. With this structure the symmetric topology is no longer satisfied.

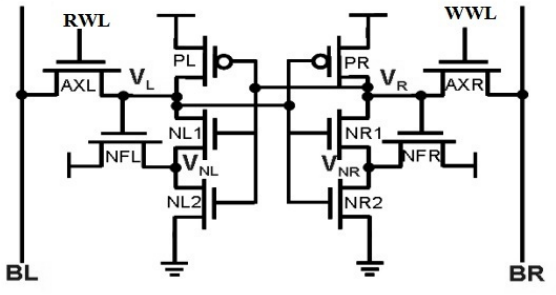

Fig. 2. Asymmetrical Schmitt Trigger Bitcell

4 Simulation Results

HSPICE simulations were performed using 45nm predictive technology model for MOS. Typical NMOS (PMOS) threshold voltage is 466mV (412mv).The conventional 6T bitcell and proposed AST bitcell are compared for various SRAM metrics. For 6T cell, transistor widths WPU/WAX/WPD are 80nm/160nm/240nm, respectively. For AST bitcell, extra transistors NFL/NL2 are of minimum width (80nm) while other transistors have the same dimensions as those of 6T cell.

The ST bitcells consumes approximately 2X area compared with the 6T cell. Hence, in order to estimate the operating conditions, it is only fair to compare the bitcells under Iso-area condition [7][10].

Fig. 3 compares the leakage current of AST with conventional 6T bitcell and ST. The results clearly demonstrate that, under Iso-area conditions, the leakage current of proposed cell is less compared to that of 6T cell and ST cell in subthreshold operation. Fig. 4 plots Iso- area power consumption vs. supply voltage (mV) of 6T, ST cell and proposed bitcell and it can be seen that the proposed AST consumes very less power compared to other in subthreshold operation making it a good choice in low power applications.

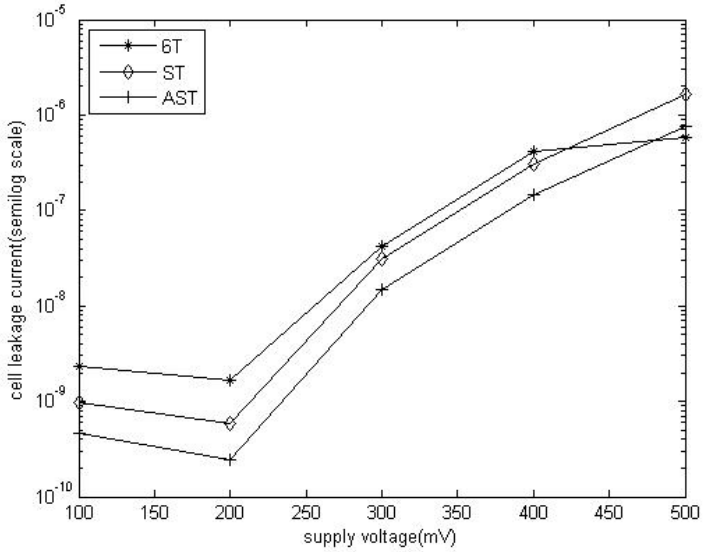

Fig. 3. Iso-area bitcell leakage current Comparison

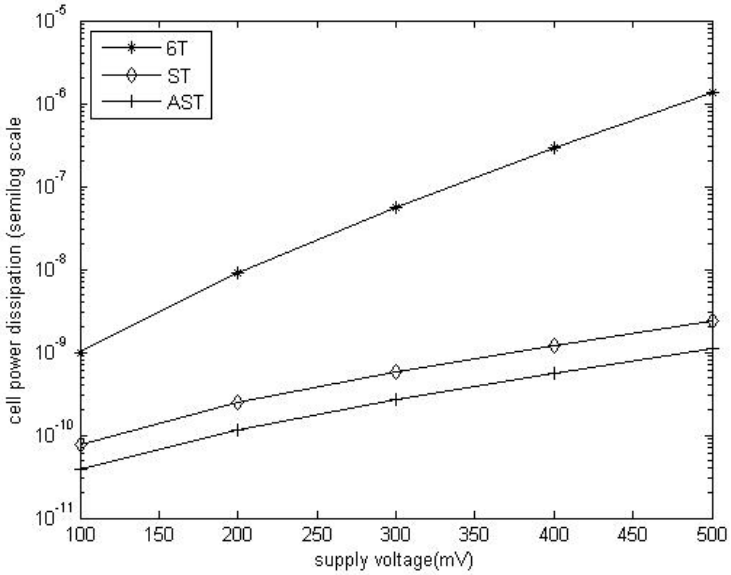

Fig. 4. Iso-area bitcell subthreshold power consumption comparison

5 Conclusions

In this work, we have proposed, Schmitt Trigger based asymmetric SRAM cell configuration that is not only robust against process variations but suitable for ultra low power applications also. The in-built feedback mechanism and asymmetry make it a suitable choice for low voltage and process tolerant operation. Asymmetrical configuration also makes this cell capable of tolerating more mismatch in neighboring transistors. Simulation results establish the effectiveness of the proposed cell.

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