POWER AWARE CHARACTERIZATION OF SEQUENCE OF INPUT VECTORS FOR STANDARD CELL BASED DIGITAL CIRCUITS

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Abstract

Minimization of power consumed by digital circuits is important for a wide variety of applications, both because of increasing levels of integration and the desire for portability. Standard cell based design approach is preferred over full custom design to achieve the short design time. One of the ways to minimize power consumed by a digital circuit is to organize sequence of its input vectors so that during transitions of input vectors, switching activity at the nodes of the circuit is minimized. We show that the problem of search of minimum power sequence of input vectors is equivalent to search for minimum weight Hamiltonian circuit in a completely connected graph, and is NP-complete. Hence, this power minimization approach is feasible for small circuits only, like standard cell based circuits. This paper proposes a heuristic to find the sequence of input vectors for standard cell based circuits such that the power dissipation is minimum. We consider layouts of small digital circuits with n inputs where 2 ? n ? 4. We use TSPICE simulations to measure switching power and total average power consumed in a circuit under consideration.

1 Introduction

An important attribute of a cell based circuit for most applications is to minimize the power consumption. The dynamic power contributes a major portion to the total power dissipation. The dynamic power dissipation in static CMOS circuits depends primarily on the number of logic transitions per unit time. As a result, the average number of logic transitions per operation can serve as the basis for comparing the power dissipation of a variety of arithmetic circuit designs. In this paper, we propose a heuristic to characterize the sequence of input vectors' transitions so that the internal switching activity and hence power in the circuit is minimized. We present results of application of the heuristic on different cell-layouts and compare them with those provided by 0-1 ILP, an exact algorithm.

2 Power estimation

An accurate estimation of power dissipation during various phases of VLSI design can verify the power dissipation requirements and thereby avoid

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complicated and expensive design changes, which might be required due to power constraint violations. The total power consumed in a circuit is composed of dynamic power, leakage power and short circuit power dissipation. We show that contribution of dynamic power to the total power in small circuits is more than 80%, rest is contributed by short circuit and leakage power. Hence, power estimation methodologies put main stress on estimation of the dynamic power. One of the simple and accurate estimation methodologies for total power computation is based on circuit simulation. Based on a given set of inputs, the power supply current can be monitored to determine the average power. Since the major part of the total power is made up of dynamic power, total power can be approximated to dynamic power; it is more true when rise time and fall time of transitions of input vectors are kept very small. For small circuits, leakage power is assumed to be negligible. Theoretically, the average dynamic power at a node in a digital circuit is given as follows.

$$P_d \ ? \ C_L . f . V_{dd}^{\ 2}$$

Where f is the frequency of operation, C_L is switching capacitor at node L, and V_{dd} is supply voltage. For aperiodic signals, the frequency of operation can be estimated by the average number of signal transitions per unit time and is represented by transition density at a node [Najm (1993)]. Due to better accuracy and small size of the circuits, we have used circuit simulation based technique to compute power dissipation in the circuit.

3 Characterizing sequence of input vector for low power

3.1 Input Pattern Pair

An input pattern pair (IPP) is defined as a pair of consecutive input signal values on input terminals as discussed in Muroyama et al (2002). For example, in a 3-input AND gate, (000, 011) characterize an IPP, which implies that input vector 000 is followed by 011. In all there would be 8 input vectors and ($^8P_2$ =) 56 IPPs for this 3-input gate. Let n denote the number of input lines and denote the number of all possible input vectors. It, then follows that number of all possible input vectors would be = 2^n and total number of IPPs would be P_2 . Here, we do not consider those IPPs, each of which is transition of a vector to itself e.g. (000,000). These types of transitions incur no power consumption.

3.2 Problem formulation

The object of the problem is to find the complete sequence of length of the input vectors resulting in minimum power dissipation in the given circuit. This sequence would start from one of the 2^n possible input vectors and end on the same. In case of a circuit with n inputs, there would be $^{2^n}P_2$ possible number of distinct input vector transitions and (-1)! number of full length sequences of input vectors transitions. We target to select the sequence for which the power consumed in the circuit is minimal. This problem can be represented by a completely connected digraph *G(V,E),* where each of the input vectors corresponds to a node i where i? V, each of the IPPs to a directed edge (i,j) where (i,j)? E, and computed power for each IPP to weight W_{ij} of the corresponding edge (i,j). Thus, a completely connected digraph with nodes and

P_2 edges can be used to represent a problem of finding minimum power sequence corresponding to n ? $\log_2$ inputs. The graph in Figure 1 corresponds to input vector transitions in a 3-input circuit. As shown in the figure there are total 56(=$^8 P_2$) edges (IPPs).

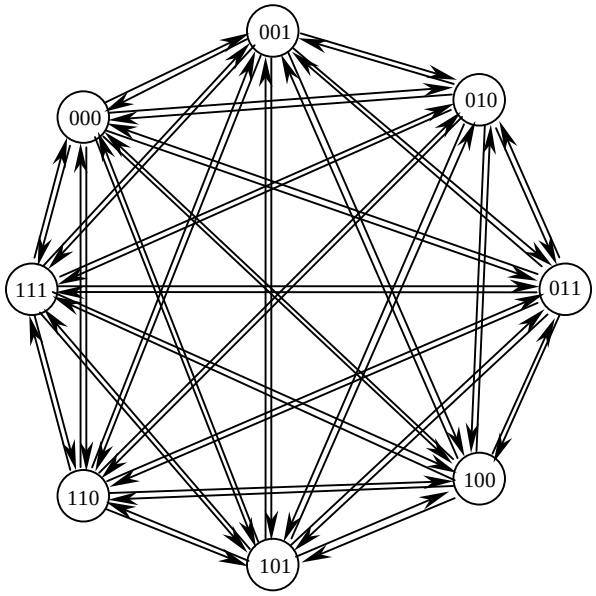

Figure 1 Possible transitions of input vectors for a 3-input circuit

The problem of finding minimum power complete length ( ) sequence of input vectors implies finding an edge cover of a given complete graph with nodes, where edge weights represent power consumed in transitions. As this sequence is a closed one, the edge cover actually corresponds to a Hamiltonian cycle. A Hamiltonian cycle is a closed path in a digraph, which starts and ends on the same node passing through all the nodes only once. The objective is to find minimum weight Hamiltonian cycle.

4 Minimum power Hamiltonian cycle

The problem of finding a Hamiltonian cycle can be mapped to an equivalent 0-1 integer linear programming (0-1 ILP) problem. ILP is an exact algorithm that provides minimum power Hamiltonian cycle deterministically. This problem is equivalent to traveling salesman problem (TSP) which is easy to describe and difficult to solve. This problem can be stated as follows.

If a traveling salesman wishes to visit exactly once each of list of cities (where the cost of traveling from city i to j is W_{ij}) and then return to home city, what is the least costly route the traveling salesman can take. The TSP problem belongs in a class of combinational optimization problems known as NP- complete.

In case of TSP, the mathematical structure is a graph where a node denotes each city and lines are drawn connecting every two nodes (called edges). Associated with every line is a distance (or cost). When the salesman can get

from every city to every other city directly, then the graph is said to be complete. When the cost of traveling from city *i* to *j* and from j to *i* is not same then TSP is called asymmetrical TSP. To formulate the asymmetric TSP on cities, let us introduce a 0-1 variable X_{ij} such that

$$X_{ij} = \begin{cases} 1 & \text{if the edge } i \text{ to } j \text{ is in tour} \\ 0 & \text{otherwise} \end{cases}$$

Every node of the graph must have exactly one edge pointing towards it and one pointing away from it, i.e., every node must have exactly one in-degree and one out-degree. These constraints alone are not enough since this formulation would allow "subtours". Subtours are disjoint loops in the same diagraph. For this reason, "sub tours elimination" constraints must be added to an ILP formulation. The ILP formulation of the Hamiltonian cycle problem can then be represented as follows.

Objective function :

$$\min \sum_{j=1}^{} \sum_{i=1}^{} C_{ij} X_{ij}$$

Such that

$$\sum_{j=1}^{} X_{ij} = 1 \quad \text{for} \quad i = 1,2.....,$$

$$\sum_{i=1}^{l} X_{ij} = 1 \quad \text{for} \quad j = 1,2.....,$$

$$\sum_{i \neq k} \sum_{j \neq k} X_{ij} \leq |k| - 1 \quad \text{for } k = 1,2....., \quad$$

$$\text{where} \quad X_{ij} = 0 \quad \text{or} \quad 1 \quad \text{for} \quad i = 1,2.....,$$

Here, k is sub-set of nodes corresponding to the edges selected. Constraints are written for $2 \leq k \leq (n-2)$. As observed from above equation set, a circuit with *n*-inputs ($=2^n$), the number of constraints is of the order of $O(2^n)$. The number of equations is large even for 3-input problem ($n=3$, $=2^3$), and it would not be feasible to write down these constraints individually for $n > 4$. The alternate is to opt for a heuristic algorithm. In this paper we propose a heuristic to solve this problem. We name this heuristic as "minimum-power edge-cover". At each iteration of its main loop, the heuristic for Hamiltonian cycle grabs a lowest weighted edge from among all remaining edges anywhere in the graph. However, the heuristic discards an edge if it could not be part of a tour with the other edges already chosen. The sub graph consisting of the edges already selected at any point in the algorithm forms a collection of simple parts. There should be no cycle *until the end* of algorithm and no vertex be incident with more than one out going and one incoming edge. The algorithm terminates when

all the edges have been processed. The algorithm is formally described in Figure 2. The worst case run time of the heuristic is about the same as for Kruskal's algorithm i.e. ? ?|E|?.

```
Minimum-Power Edge-Cover G (V, E)
1.      R=E;  // R is remaining edge
2.      C=?;  // C is cycle edge
3.      While R is not empty
3.1             Remove the shortest edge (v, w) from R
3.2             Check for cycle and in/out degree of a node
3.3             If  [(v,w) does not make a cycle with edges in C]
                    AND
                    [(v,w) would not be second out going or second incoming
                            edge in C incident on v or w]

3.3.1                       Add (v, w) to C
3.4             Continue loop
4.      Add the edge connecting the end points of the path in C
5.      Return C;
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Figure 2 Minimum-power edge-cover algorithm

5 Results

We have considered layouts of small digital circuits e.g. 2-input NAND, XOR, 2to1 MUX, full adder, S-R FF, and AOI221 in 0.5?m static CMOS technology using NAND implementation only. The layouts were extracted into SPICE; with proper parasitic attached to the desired nodes, each circuit was simulated for all possible IPPs and the power information was obtained for each of the IPPs. For these circuits, our tool based on heuristic provided minimum power as well as maximum power sequence of input vectors. The results thus obtained were verified with those obtained using ILP for circuits with n ? 3. It can be observed in Table 1 that the dynamic power is the main constituent of the total power dissipation. It forms more than 90% component of total power. We have considered very small values for rise time (RT) and fall time (FT) of input waveform so that short circuit power is negligible. Table 2 shows the optimal sequence for minimum power found using 0-1 ILP. The results using minimum-power edge-cover heuristic are shown in Table 3. We observe that the results are nearly optimal, i.e., power consumed by two sequences provided by ILP and heuristic are almost same. The sequences that incur maximum power were also obtained using same heuristic, and are illustrated in Table 4. In case of S-R FF we did not use prohibited input vector (0,0) while searching for sequence of input vectors for low power.

Table 1 Total power versus Dynamic power

Cell	Total Power	(Dynamic + Leakage) Power	Dynamic Power as % of total power
	***RT = 0.1ns *FT = 0.1ns**	***RT = 0.01ns *FT = 0.01ns**	
XOR	328 ?w	325 ?w	99.08 %
NAND	37 ?w	35 ?w	94.59 %
2_1 MUX	211 ?w	202 ?w	95.73 %

**RT= rise time, *FT = fall time*

Table 2 Minimum power sequence using ILP

Cell	*Min. power input vector sequence*	*Power (? W)*
XOR	3, 0, 2, 1	257
NAND	2, 0, 1, 3	28
S-R FF	2, 1, 3	161

Table 3 Minimum power sequence using proposed heuristic

Cell	*Min. power input vector sequence*	*Power (? W)*
XOR	3, 0, 2, 1	257
NAND	0, 1, 2, 3	35
2_1 MUX	2, 6, 0, 4, 1, 3, 7, 5	87
ADDER	6, 7, 0, 1, 4, 2, 3, 5	2160
S_R FF	2, 1, 3	161
AOI	15, 13, 6, 3, 2, 7, 11, 9, 12, 0, 10, 8, 1, 4, 5, 14	85

Table 4 Maximum power input vector sequence

Cell	*Max. power input vector sequence*	*Power (? W)*
XOR	1, 0, 3, 2	328
NAND	3, 1, 0, 2	37
2_1 MUX	1, 6, 3, 4, 7, 2, 7, 5	211
ADDER	0, 3, 6, 5, 2, 7, 4, 1	2465
S_R FF	3, 1, 2	305
AOI	5, 12, 4, 8, 3, 11, 2, 10, 9, 1, 7, 6, 13, 14, 15, 0	106

6 Conclusion

In this paper, we have proposed a heuristic to find the sequence of input vectors in the standard cell based circuits such that the power dissipation is minimized. Experimental results illustrate that the sequences obtained using heuristic are nearly optimal or optimal. This work can be extended to larger circuits to find out the sequence of input vectors incurring minimum power. This approach can be combined with the approach in Muroyama et al (2002) for large circuits. Our approach can be used in organizing input vectors for minimum power for the gates and modules of the main circuit that are directly connected to inputs. For the gates and modules lying inside cone of an output, i.e., between the modules connected to the inputs and the final output, power minimization can be achieved using the approach of Muroyama et al (2002).

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