A Study of Low Power Design Techniques for Application Specific Processors

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Abstract

Power becomes a critical constraint for designing embedded systems. Designing for low power becomes increasingly important in many applications like wireless telephony, mobile computing, high performance computing and high-speed networking. The increasing popularity of power constrained in embedded computing applications drives the need for analyzing & optimizing power in all components of a system.

The power can be analyzed at different levels of abstractions such as architectural, logic, layout and device level. Architectural Level is most amenable to power optimization among all [1]. Hence this paper concentrates mostly on the architectural level power estimation and optimization. At architectural level, the major part of the power consumption takes place in components viz. CPU, Bus and cache. This paper studies the efforts in literature focusing on the estimation and optimization of these power components by developing (i) a power model and (ii) optimization of power, for each of the components.

The paper presents the estimation and optimization of CPU power by using software power estimation and optimization techniques [5,6]. The bus power consumption can be classified in two parts i.e. data buses and addresses buses. For data/address buses, encoding techniques can optimize the bus power. Bus encoding transition signaling (BITS) [3] and (half identity half-reverse transition signaling (hihrTS) [3] encoding techniques for data buses and Partial bus invert (PBI) [4] for address buses are illustrated for optimizing data bus power.

The paper also presents the estimation and optimization techniques for cache. Finally the system level power saving methods are discussed employing techniques such as clocking gating; sub-system power down schemes- static and dynamic power-off; and dynamic voltage scaling.

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