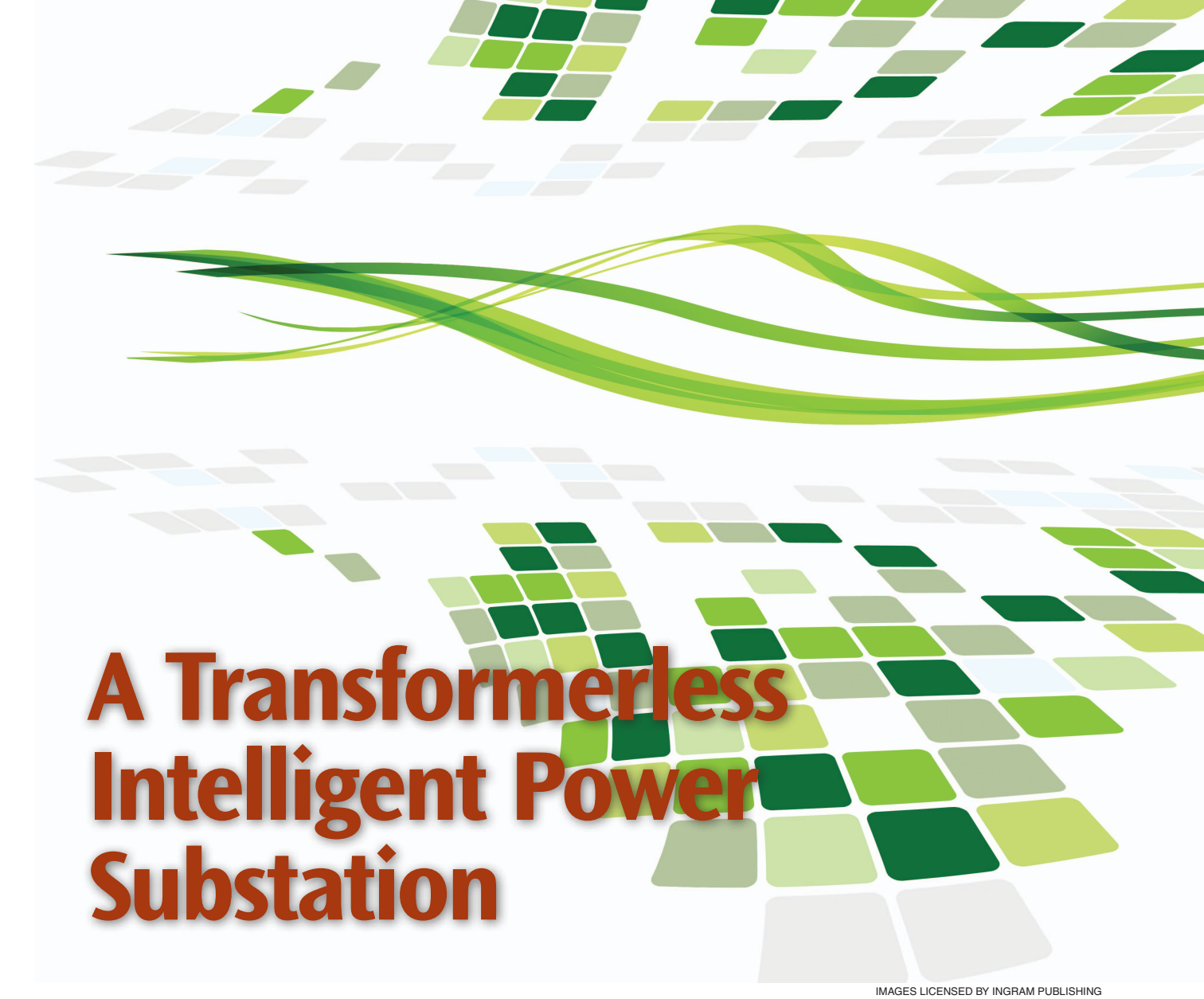
A Transformerless Intelligent Power Substation



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A three-phase SST enabled by a 15-kV SiC IGBT

by Krishna Mainali, Awneesh Tripathi, Sachin Madhusoodhanan, Arun Kadavelugu, Dhaval Patel, Samir Hazra, Kamalesh Hatua, and Subhashish Bhattacharya

The solid-state transformer (SST) is a promising power electronics solution that provides voltage regulation, reactive power compensation, dc-sourced renewable integration, and communication capabilities, in addition to the traditional step-up/step-down functionality of a transformer. It is gaining widespread attention for medium-voltage (MV) grid interfacing to enable increases in renewable energy penetration, and, commercially, the SST is of interest for traction applications due to its light weight as a result of medium-frequency isolation. The recent advancements in silicon carbide (SiC) power semiconductor device technology are creating a new paradigm with the development of discrete power semiconductor devices in the range of 10–15 kV and even beyond—up to 22 kV, as recently reported. In contrast to silicon (Si) IGBTs, which are limited to 6.5-kV blocking, these high-voltage (HV) SiC

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devices are enabling much simpler converter topologies and increased efficiency and reliability, with dramatic reductions of the size and weight of the MV power-conversion systems.

This article presents the first-ever demonstration results of a three-phase MV grid-connected 100-kVA SST enabled by 15-kV SiC n-IGBTs, with an emphasis on the system design and control considerations. The 15-kV SiC n-IGBTs were developed by Cree and packaged by Powerex. The low-voltage (LV) side of the SST is built with 1,200-V, 100-A SiC MOSFET modules. The galvanic isolation is provided by three single-phase 22-kV/800-V, 10-kHz, 35-kVA-rated high-frequency (HF) transformers. The three-phase all-SiC SST that interfaces with 13.8-kV and 480-V distribution grids is referred to as a *transformerless intelligent power substation* (TIPS). The characterization of the 15-kV SiC n-IGBTs, the development of the MV isolated gate driver, and the design, control, and system demonstration of the TIPS were undertaken by North Carolina State University's (NCSU's) Future Renewable Electrical Energy Delivery and Management (FREEDM) Systems Center, sponsored by an Advanced Research Projects Agency-Energy (ARPA-E) project.

Background

Si-based power semiconductor devices have been widely used for several decades over a wide range of voltage and power levels [1]. Si power devices have almost hit the theoretical limits in terms of their voltage rating and switching capabilities. The HV Si IGBTs are typically limited to 6.5 kV, with a switching frequency less than 1 kHz [2]. These limitations pose challenges in the MV applications of Si IGBT-based power converters due to either the required series connection of the IGBTs or the complex multilevel converter topologies resulting in relatively inefficient and bulky systems.

Due to its much higher critical electric field, better thermal conductivity, and higher temperature capability in comparison to Si, 4H-SiC has been found to be a viable alternative in its two-decade-long development [3]. An SST application based on the series connection of 1,500-V SiC JFETs (super cascode), with a dc-link voltage of 5 kV, has been presented by ETH Zurich [4]. The challenge in the series connection of LV devices lies in the complex static and dynamic voltage balancing across each single device. In recent years, fast-switching (>5 kHz) SiC MOSFETs up to 15 kV [5] and SiC IGBTs beyond 20 kV have been developed [6]. The 10-kV SiC MOSFETs have been demonstrated on a single-phase 1-MVA soft-switched solid-state power substation by General Electric in 2011 [7]. The 13-kV SiC MOSFETs have been demonstrated on a 20-kVA single-phase SST by the FREEDM Systems Center [8]. The objective of this article is to present the first-ever SST demonstration of SiC 15-kV IGBTs by developing a three-phase SST capable of interfacing a 13.8-kV distribution grid with an isolated 480 V load or grid connection.

The proposed three-phase SST topology, as shown in Figure 1, is referred to as a TIPS [9] and interfaces the three-phase, 13.8-kV and 480 V distribution grids. The TIPS has three power-conversion stages. The active front-end

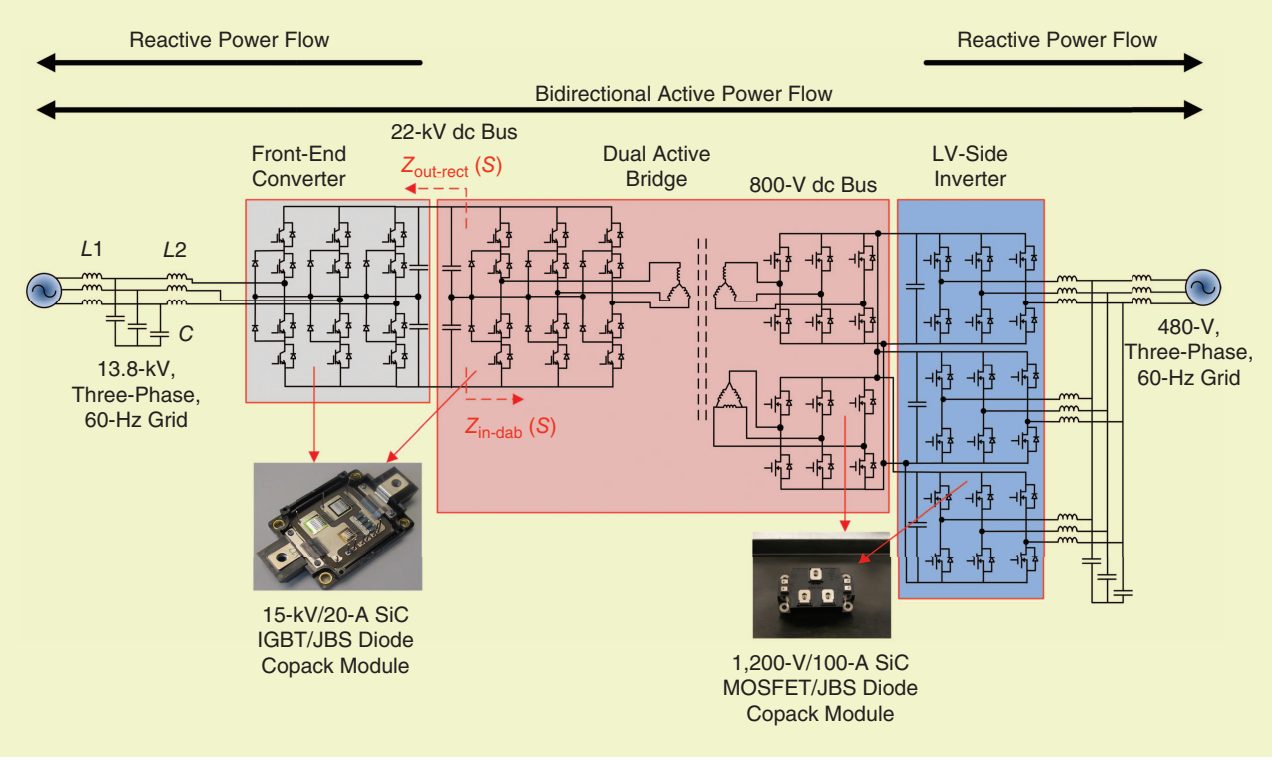

FIG 1 A schematic of the TIPS—a 13.8-kV to 480-V grid-interfaced three-phase SST [30].

converter (AFEC) is tied to an MV 13.8-kV distribution grid with a three-level neutral point clamped (3L-NPC) converter built using the 15-kV SiC IGBTs. It is a PWM boost rectifier with a 22-kV dc bus on the output, and it is operated with hard-switched sine-triangle pulsewidth modulation (SPWM) at 3–5 kHz. The AFEC dc bus (22 kV) is converted to a LV-side dc bus (800 V) using an HF dc-link, enabled by a three-phase dual active bridge converter (DABC) [10].

The DABC is responsible for isolation and voltage conversion in the TIPS system. The DABC is a zero-voltage switching (ZVS) soft-switched converter operated at 10 kHz. The MV side of the DABC is also a 3L-NPC converter built using 15-kV SiC IGBTs, and the LV side has a 1,200-V SiC MOSFET half-bridge modules-based two-level (2L) converter for each star- and delta-connected secondary winding. The output LV inverter stage is developed using 1,200-V SiC MOSFET modules with three interleaved 17–20-kHz, 35-kVA converters.

15-kV SiC n-IGBT Characterization

The 15-kV SiC n-IGBTs were developed by Cree for the first time, sponsored by an ARPA-E program. The TIPS is chosen as a platform for demonstration of the 15-kV SiC IGBT as it enables integration of a 13.8-kV, three-phase grid with a simple three-level converter topology. Figure 2 shows the copack module developed by Powerex for the 15-kV SiC IGBT, with two 10-kV SiC junction barrier Schottky (JBS) diodes (in series), current-sensing resistors, and a thermistor for temperature measurement. The active area of the 15-kV SiC n-IGBT is 0.32 cm^2, with a total chip area of 8.4 mm × 8.4 mm. It is a punch-through device with a drift thickness of 140 μm, as shown in Figure 3. Two different 15-kV SiC IGBT designs with field-stop buffer layer thicknesses of 2 and 5 μm have been evaluated for TIPS application.

Understanding the behavior of state-of-the-art SiC IGBTs is very critical for the development of the MV TIPS. Therefore, a double-pulse test setup was built to characterize SiC

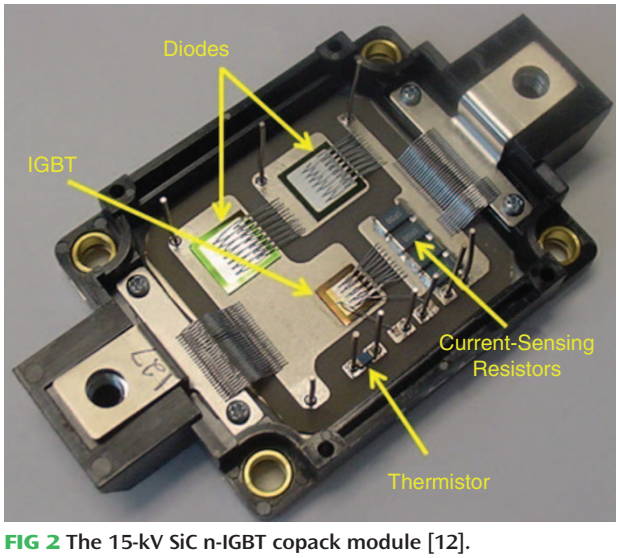

FIG 2 The 15-kV SiC n-IGBT copack module [12].

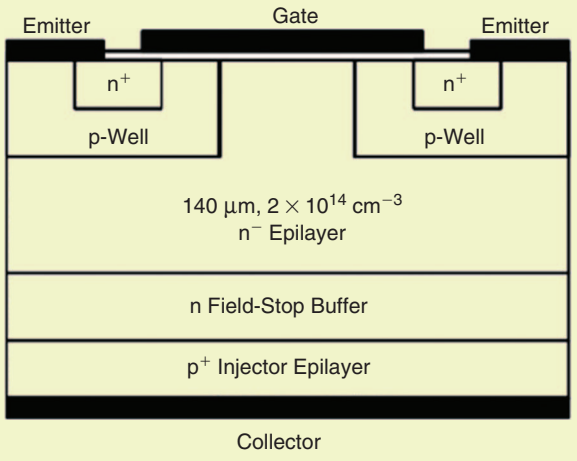

FIG 3 A simplified cross-sectional view of the 15-kV SiC n-IGBT.

IGBTs up to a 11-kV dc voltage and a junction temperature of 175 °C [11], [12]. Both turn-on and turn-off switching transients exhibit distinct two-phase voltage transitions due to the deep punch-through design of the IGBT. The forward drop is increased by about 15% with a temperature rise from 25 to 150 °C. However, the turn-off switching loss is increased by a factor of two from 25 to 175 °C due to increased injection from the backside p^+ layer at elevated temperatures. The turn-off switching transition duration at 10 kV, 10 A, and 175 °C is about 800 ns for the 5-μm buffer layer IGBT, with negligible tail current. The turn-off switching loss (at 25 °C) at for 5-μm IGBT is 7.2 mJ, whereas it is 20.4 mJ for a 2-μm IGBT. On the other hand, the 5-μm buffer layer IGBT has a forward drop of 7.2 V, whereas it is 6.0 V for the 2-μm buffer layer IGBT at 20 A and 25 °C. The SiC IGBTs have extremely fast switching transients, with turn-on dv/dt around 100 kV/μs over the punch-through voltage range. Figure 4 shows a comparison of the 2- and 5-μm IGBT turn-off transient at 10 kV, 10 A, and 25 °C, where it is evident that the 5-μm IGBT

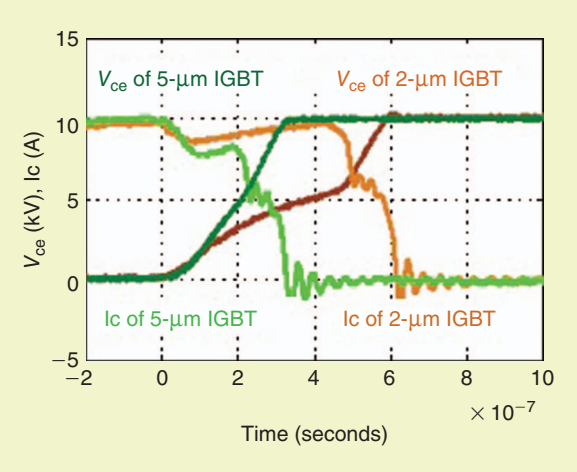

FIG 4 The turn-off transitions of a 15-kV, 2- and 5-μm-thick buffer layer, SiC IGBT at 10 kV, 10 A, and 25 °C with $R_{G(OFF)}$ of 10 Ω.

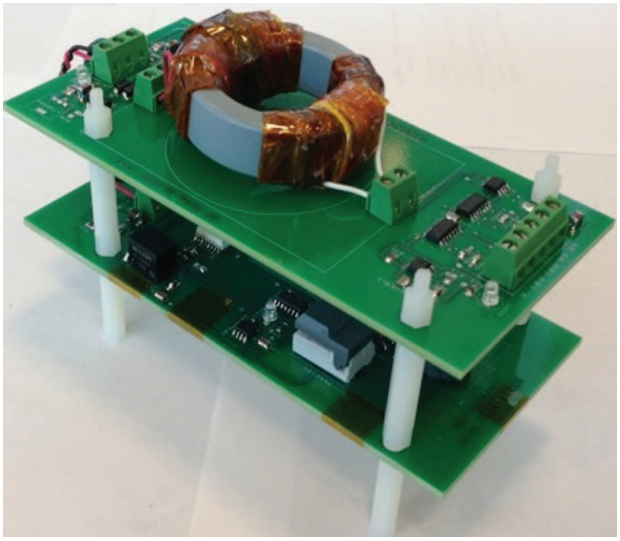

FIG 5 The HV isolated gate driver prototype for the 15-kV SiC IGBT [15].

has a much faster transition. A detailed analysis of dv/dt of both the 15-kV SiC IGBTs is presented in [13].

MV Gate Driver

Commercially available gate driver isolation power supplies have a maximum dielectric test voltage (50 Hz, 1 minute) of 18-kV root mean square (rms) [14]. These power supplies are meant for application in 6.5-kV Si IGBT-based multilevel converters, where the dv/dt values and switching frequencies are expected to be at least an order of magnitude lower than that of the 15-kV SiC IGBTs. The 15-kV SiC IGBTs present a completely different scenario, with dv/dt greater than 100 kV/μs and with an operating dc voltage up to 11 kV as well as a high switching frequency (5–10 kHz), which will require significant derating for the reliable operation of the gate driver. This required in-house development of the gate driver, with a parasitic interwinding coupling capacitance of 3.4 pF at 50 MHz to handle such high dv/dt stress. The 11-kV, high-dv/dt gate driver prototype is shown in Figure 5.

The validation of the gate driver in HV, hard-switched, HF, high-dv/dt test circuits is another critical element. The gate driver was evaluated on boost-fed-buck converter and buck-boost converter topologies to expose the gate driver to high-side voltage and dv/dt (over 100 kV/μs at 11-kV dc) as well as voltage swings from −2 to +8 kV [15]. In addition, the electromagnetic interference (EMI) robustness was validated by probing several signals and V_{cc} of different ICs on the gate driver power supply [15].

Modular 3L-NPC Converter for TIPS

Based on the switching loss measurements, the hard-switching frequency limits of the 15-kV SiC IGBT were evaluated and demonstrated on a 10-kV dc–dc boost converter [10]. It was found that the high thermal resistance of the module package is pivotal in determining the SiC IGBT thermal limits. The thermal resistance was found to be 0.49 °C/W from the junction to the top of the heat sink. The 3L-NPC converter design and demonstration results with 10-kV dc input are presented in [16].

The 3L-NPC converters on the MV side of the TIPS have a modular structure with three poles for the AFEC stage and three poles for primary side of the DABC. Each 3L-NPC pole has its own dc-link capacitor with a bus-bar connection to the 15-kV SiC IGBTs and 20-kV (2 × 10 kV) SiC JBS clamping diodes for low stray inductance. The poles were individually tested up to 10-kV dc input in inverter mode at 5 kHz and 7.5 kW before integrating them into the three-phase TIPS. Figure 6 shows a 3L-NPC pole mounted on HV bushings for reducing common-mode currents. The PWM signals are transmitted optically to minimize EMI issues and provide higher voltage isolation as well as controller operation distant from the TIPS 3L-NPC converter poles.

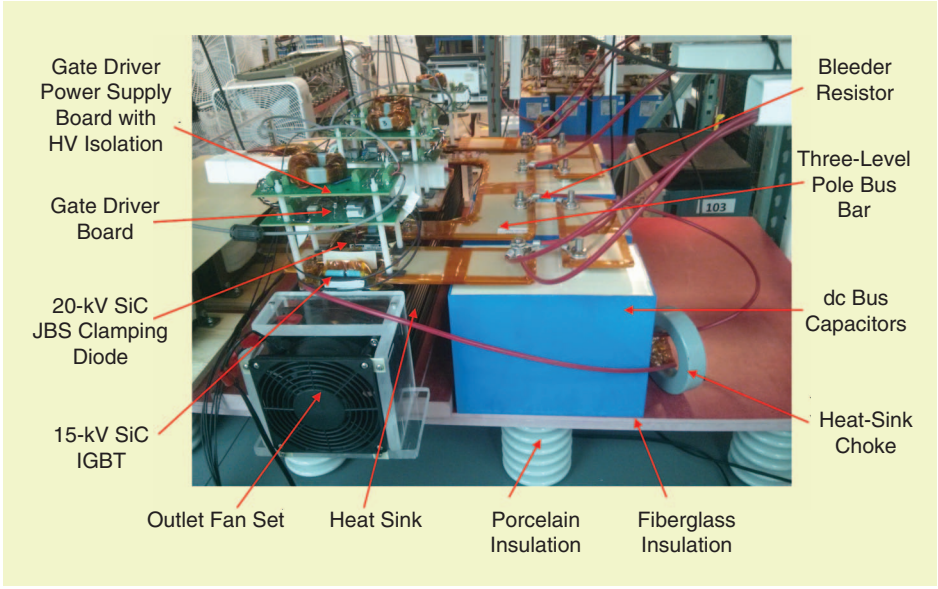

FIG 6 A pole of a 3L-NPC converter [31].

Active Front-End Converter

The AFEC is a critical stage of the SST. It handles many functions, including unity-power-factor (UPF) operation, power-factor control, regulating the MV dc bus, grid-side power-quality improvement, and var compensation. With higher switching frequencies of 3–10 kHz possible with HV 10–15-kV SiC devices, the filter inductance can be as low as

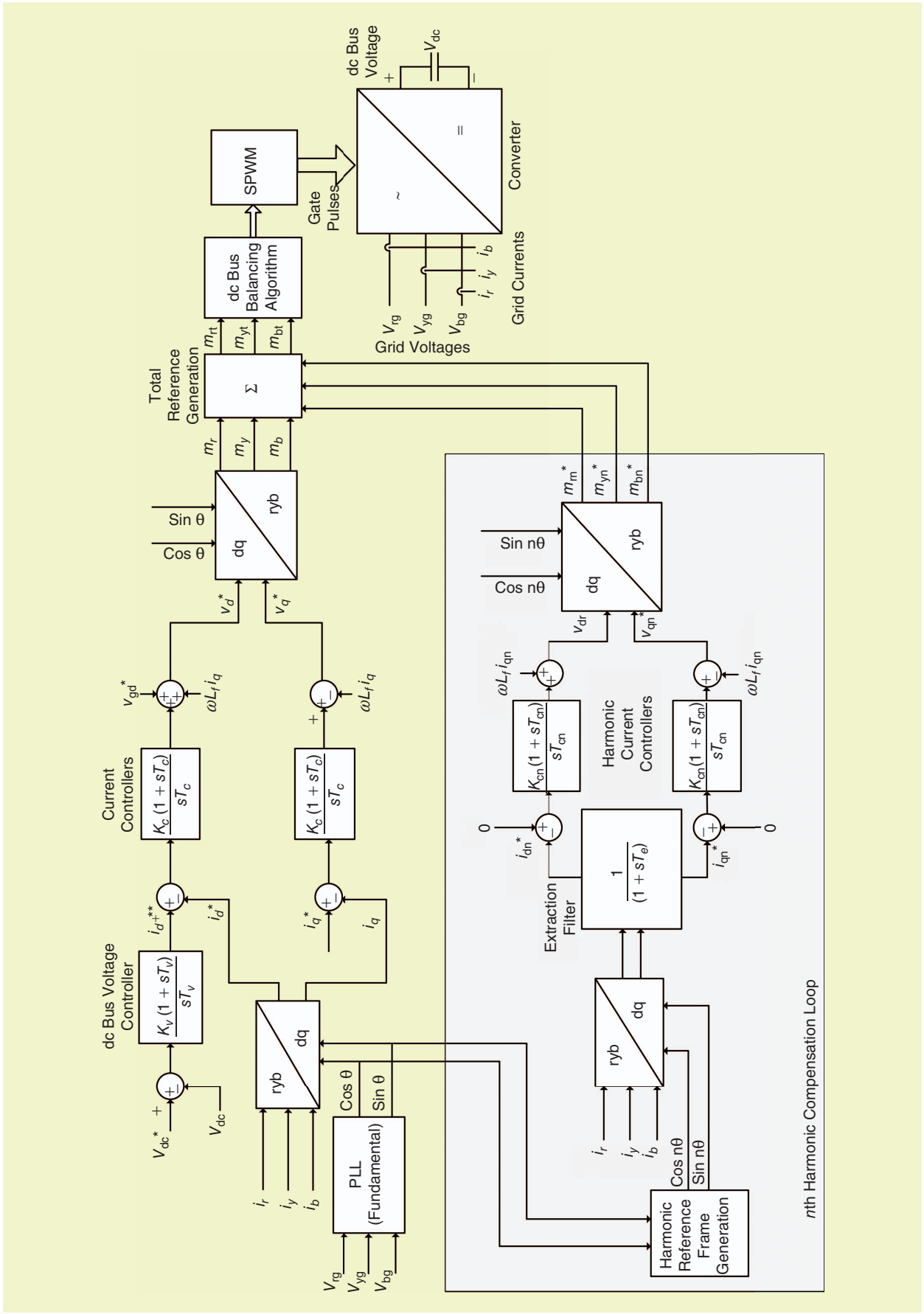

FIG 7 A block diagram of the AFEC converter control with grid-side harmonic reduction.

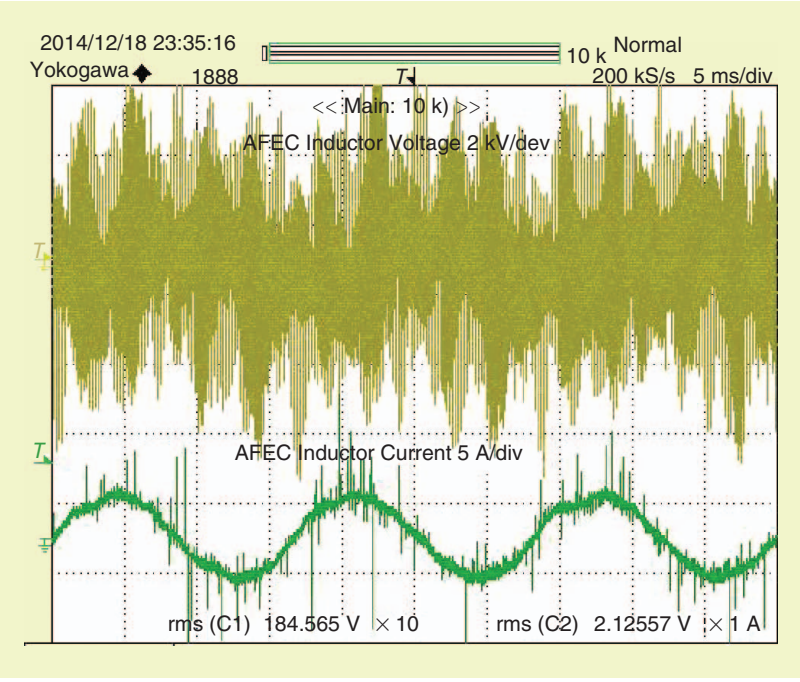

FIG 8 Experimental waveforms of the AFEC inductor at 3.6-kV grid-tied operation at 8 kW.

0.05 p.u. (440 mH for a TIPS AFEC with a 22-kV dc bus, 3-kHz switching ripple, and 100 kVA). The size and rating of filter inductance can be further reduced using an *LCL* filter. For TIPS AFEC, the total filter inductance is designed for 3% of the grid voltage (13.8 kV). This is distributed in the ratio of 1:2 in between the grid-side inductor (L_1) and converter-side inductor (L_2). This results in 90 mH for L_1 and 180 mH for L_2 [17]. The converter-side inductor (L_2) should be designed to withstand the 3-kHz switching ripple. To reduce core losses, the core material is required to be either ferrite or nanocrystalline. The AFEC input filter capacitor value is then decided based on the desired resonant frequency. The choice of resonant frequency should be made carefully as the switching frequency is only 3 kHz. It needs to be reasonably lower than 3 kHz to eliminate the switching ripple. Also, it cannot be too close to the dominant lower-order harmonics, like the fifth and seventh, to prevent harmonics being amplified in the supply [18]. Thus, an optimum value of 1 kHz is selected for filter resonance frequency design. This results in an *LCL* filter capacitance value of 0.42 μF.

The complete AFEC control system is shown in Figure 7. Synchronous frame *d*–*q* vector control is used with the grid voltage vector as the reference. The *d*-axis control loop is responsible for controlling the dc bus voltage. There are two proportional-integral controllers in the *d*-axis: the inner current loop controller and the outer MV dc bus voltage loop controller. In the *q*-axis, only one current controller is used with its reference set based on the grid reactive power requirements. The AFEC control under unbalanced grid conditions and dc bus midpoint shift issues are addressed. The TIPS AFEC is designed to handle MV (13.8 kV) at relatively low power levels of 100 kVA when supplying power to the grid or supplying loads during nonpeak hours. This requires good bandwidth current control implementation at low-current levels (4.2 A rms). MV transitions across the 15-kV SiC IGBTs and the associated higher deadtime requirements (of 3.8 μs) lead to new challenges in harmonic elimination. The controller design and implementation for the AFEC stage of TIPS is discussed in detail in [19]. At startup, huge inrush currents will be drawn from the grid to charge the MV dc bus capacitors. The startup inrush currents are limited to safe values for the 15-kV SiC IGBTs by precharging the MV dc-link voltage from the LV side, and this startup procedure is presented in [20].

Figure 8 shows the experimental inductor waveforms for the AFEC. The AFEC is operating at 7-kV dc bus voltage, 3.6-kV ac input grid, hard-switching at 5 kHz, and delivering 8-kW power to the load. The inductor used in the scaled-down voltage demonstration is 140 mH (2 p.u. at the operating conditions). The grid-tied Variac and step-up transformer used for the experiments contributes another 30 mH as leakage inductance. The inductor completely supports the entire ripple voltage generated by the AFEC across it.

Dual Active Bridge Converter

The DABC is operated by switching two sets of converters in 10-kHz square-wave PWM mode, feeding the primary and secondary side of an HF transformer. The DABC power flow is controlled by the phase shift between the primary and secondary voltages, the magnitude of the voltages, and the leakage inductance of HF transformer. The full-load DABC angle is selected as 45°, where the ideal *P*/*Q* ratio is 1.2, keeping in view that a large reactive power results in higher conduction losses. Also, a smaller full-load DABC angle makes the phase control resolution small and results in higher current distortions. The DABC requires high *Q*-factor series inductance for power transfer and smooth power flow and current controllability. The MV-side converter of the DABC is a three-phase (or three poles of) MV 3L-NPC converter. The LV side consists of a pair of 2L, three-phase, 1,200-V/100-A SiC MOSFET converters; the two converters share the rated load of 100 kVA. The LV converters are connected to three single-phase transformers in a star–delta configuration. In this configuration, the two converters operate with a mutual phase shift of 30° to produce a synchronous fundamental at the switching frequency of 10 kHz. This dual winding arrangement is a preferred solution to reduce harmonics for better performance, as well as power flow and current control [9]. The 3L-NPC converter is operated with 41% duty ratio to generate a nearly sinusoidal primary current in the HF transformers. The challenges for designing MV DABCs are HF

transformer compactness (power density, size, weight, and volume) versus parasitics capacitance optimization/minimization, maintaining ZVS and low reactive power flow for higher efficiency, EMI considerations for smooth current control, flux-saturation protection, and midpoint voltage balancing of 3L-NPC converter poles are reported in detail in [21]. The design considerations and operation of such MV HF transformers are addressed in [22]–[24].

Figure 9 shows a photo and the HF equivalent circuit of the MV transformer designed for the TIPS DABC. The design of this transformer and extractions of the model parameters are presented in [24]. The output LV dc bus has a voltage sensor for feedback control. There are two MV voltage sensors connected to 3L-NPC midpoint voltages on the HF transformer primary side. The 3L-NPC midpoint voltages need to be balanced by feedback control since the nonidealities and dead times might make it unbalanced even if the PWM control signals are balanced [25]. This is done in control by adjusting the positive and negative time periods of a switching period. The primary-side transformer currents are also sensed for feedback. A field-programmable gate array-based control platform using an ultrafast 12-bit parallel analog-to-digital converter with a sampling rate of 2 megasamples/second is implemented. A synchronous frame d–q-based inner current control loop enables fast response and provides another level of overcurrent protection [25], [26]. The midpoint dc bus voltage balancing is achieved through feedforward control.

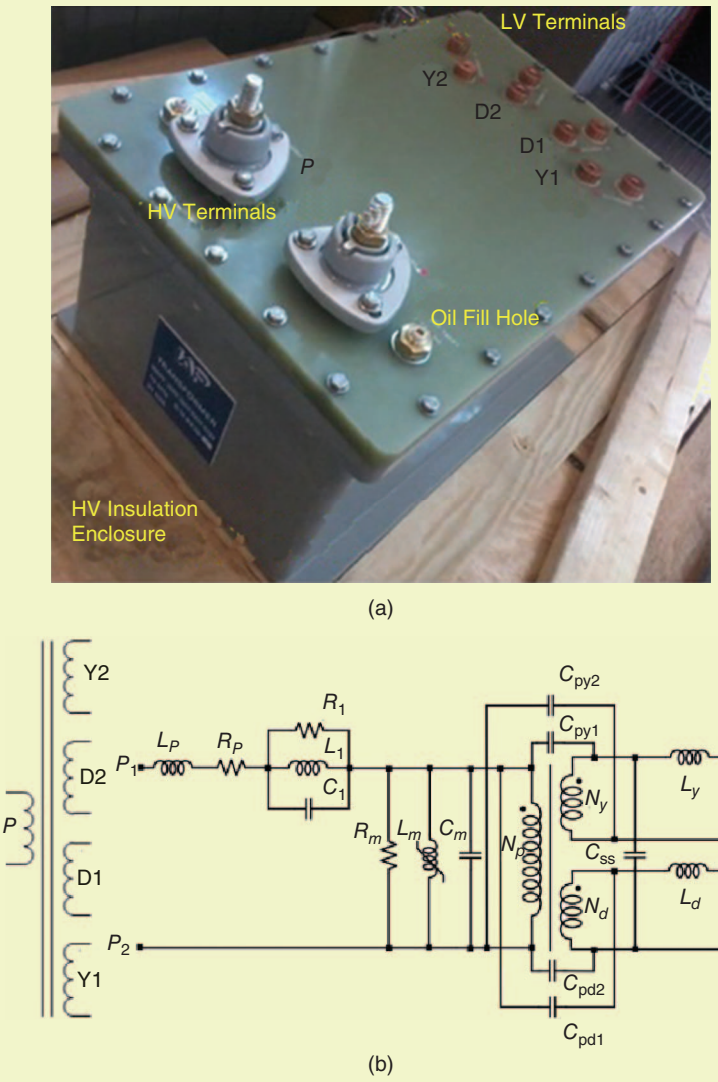

FIG 9 An HF MV DABC transformer rated 22 kV/800 V, 10 kHz, and 35 kVA: (a) the transformer and (b) an equivalent circuit model of the HF transformer [24].

Figure 10 shows the experimental waveforms of the DABC operation with 6-kV input and 400-V output at 7.4-kW and 10-kHz switching frequency. For each DABC pole voltage and current waveform, one phase is shown in Figure 10. The LV dc-output supplies a resistive load. The MV primary-side current shows considerable ringing; this is caused by interaction of transformer parasitics capacitance with the high dv/dt (up to 100 kV/μs) of 15-kV SiC IGBT switchings. The ringing can be lowered by reduction of parasitics capacitance by HF transformer design and also by lowering the 15-kV SiC IGBT switching dv/dt by increasing gate driver resistance. The first option will increase the size of the HF transformer, and the second option will increase switching losses. As a more viable solution, external MV primary-side dv/dt filters are used for attenuating the ringing. Additional tie inductors are used on both the secondary LV sides to reduce circulating current between star- and delta-connected converters. This ringing in the currents reduces the available DABC ZVS range.

The 3L-NPC converter is operated with 41% duty ratio to generate a nearly sinusoidal primary current in the HF transformers.

For ZVS operation, the MV converter current must lag its pole voltage, and for the secondary LV converter, it must lead. Smaller magnetizing inductance helps DABCs to achieve ZVS operation, albeit with efficiency penalty as it causes increased reactive power-flow resulting

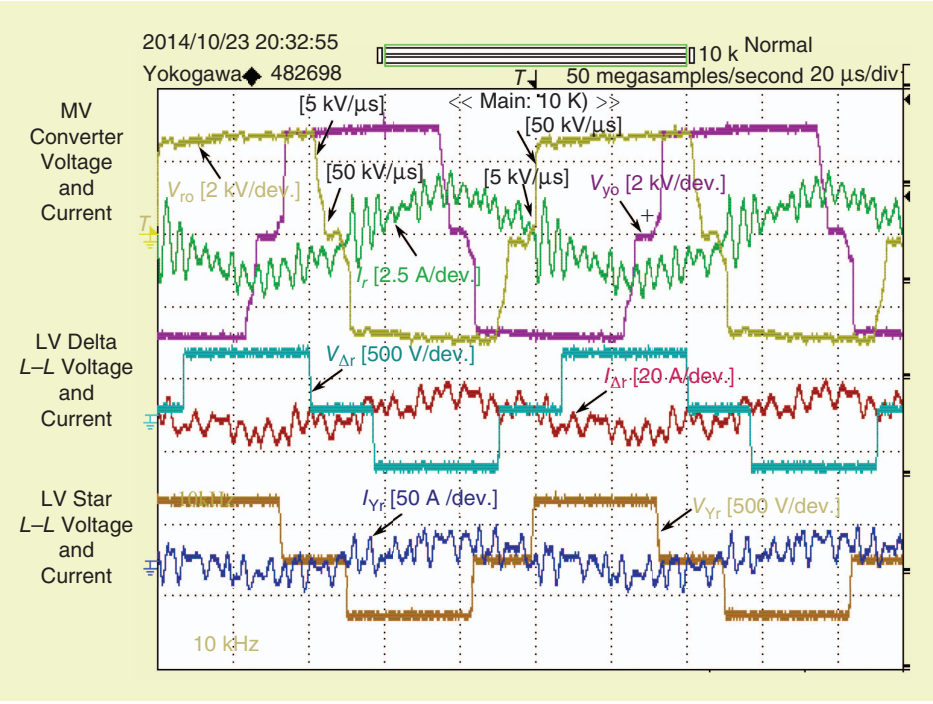

FIG 10 Experimental waveforms of DABC operation at 6 kV to 400 V, 7.4-kW, and 10-kHz switching frequency.

in increased conduction losses. Since the DABC angle is dependent on load current, at light loads the DABC might lose ZVS operation. Losing ZVS operation causes hard-switching with steeper voltage rise during turn-on, resulting in further increased ringing. When ZVS occurs, the antiparallel diodes carry current to discharge the device voltage smoothly to zero. For this, the dead time must be higher than the discharge time. At light load conditions, this requirement can be difficult to achieve since the 15-kV SiC IGBT with SiC JBS diode copack module has considerable capacitance. The discharging current depends on the DABC loading and the phase lag of the current. Hence, the maximum switching frequency for the DABC with the 15-kV SiC IGBT devices depends on the dead time along with switching losses. The device (or total module) capacitance helps to achieve ZVS during turn-off, but it necessitates larger dead time for ZVS operation during turn-on.

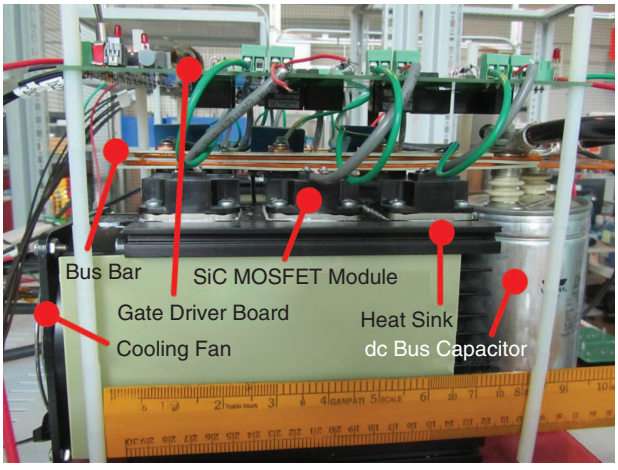

FIG 11 The 1,200-V, 100-A, SiC half-bridge MOSFET module-based three-phase, 2L voltage source converter [28].

LV-Side 1,200-V SiC MOSFET-Based Converters

Three-phase converters (2L) for the LV side of the DABC and the inverter stage for 480-V grid interface are built with 1,200 V, 100-A SiC MOSFET half-bridge modules packaged by Powerex with dies from Cree. The *V–I* characteristics of the 1,200-V SiC MOSFET and its antiparallel JBS diodes are given in [27]. Hard-switching characterization of these 1,200-V SiC MOSFETs is performed to evaluate their turn-on and turn-off switching behavior. Switching loss is measured as the function of switch current at different junction temperatures and gate resistances. Also, the switching dv/dts are characterized with varying gate resistances to select a suitable gate resistance to limit dv/dt to 15 kV/µs. With the experimentally evaluated switching energy loss data, the cooling system of the converters and its packaging are designed.

The gate driver is designed to provide high peak current (up to 15 A if required) and shoot-through capability tested up to 1-kV dc bus voltage. Since these gate drivers handle relatively low dv/dt (in the range of 15 kV/µs) compared to the MV-side gate drivers, commercially available isolated dc–dc converters are used for isolated gate driver power supply. The packaged three-phase 2L converter is shown in Figure 11. All components of the converter, including the 1,200-V, 100-A modules, sandwiched dc bus bar, gate drivers, heat sink with forced-air cooling system, and dc bus capacitor are shown in Figure 11. Each converter has been demonstrated up to 50 kVA at 20-kHz switching frequency and 800-V dc bus voltage [28]. The converter test results at 35-kVA operation are shown in Figure 12.

TIPS System Integration

The three stages of the TIPS systems are integrated together, as shown in Figure 1. Appropriate start-up sequences and coordination between the three stages have been established. If any of the DABC gate drivers generate fault signals, they are communicated optically to other converters (AFEC, LV-side inverters) to smoothly initiate the shut-down process. The AFEC fault signal

turns off the DAB's LV-side converters so that it runs in open-loop dc–dc mode to safely discharge the MV DAB-side dc bus voltage. The MV DABC generated fault signal turns off the AFEC so that it does not see a load rejection since it is operated as a boost converter system. Also, faults on the LV inverters are communicated to the DABC and AFEC converters. The layout of the converters and the wiring system has been designed carefully to avoid noise-pick-up loops. All control feedback wires and gate power-supply wires are shielded and grounded.

The stability of the closed-loop controlled systems in cascade, such as in the TIPS system, is very critical. Three individual subsystems are cascaded to make the TIPS system, and, therefore, stability at each interface between the subsystems needs to be ensured. A total dc bus capacitance of 90 μF is considered for the AFEC. With this relatively small dc bus capacitance and energy storage, the AFEC may have instability issues when connected to an active load such as the DABC. For stable operation of any cascaded converter systems, the closed-loop output impedance of the AFEC should be lower than the closed-loop input impedance of the next stage DABC for all frequencies [29]. This will ensure that the two subsystems are totally decoupled and the control systems of the two subsystems do not interact with each other. If either the transferred power increases or the dc bus voltage increases, the modulation index of the AFEC is reduced, and the output impedance of the AFEC increases. Similarly, if the power transferred increases, the phase angle of DABC increases and its output impedance reduces. Therefore, it is necessary to meet the stability criteria throughout the operating range of dc bus voltage and power transferred for the TIPS system.

The TIPS system is run in the integrated mode. The AFEC and DABC are integrated at 7-kV bus voltage with 8-kW load. The ac grid-tied voltage is 3.24-kV line-to-line rms. The DABC LV side is regulated at 420 V. Figures 13 and 14 show the AFEC and DABC waveforms, respectively, under the integration mode. These waveforms also indicate that the interaction between the AFEC and DABC is stable.

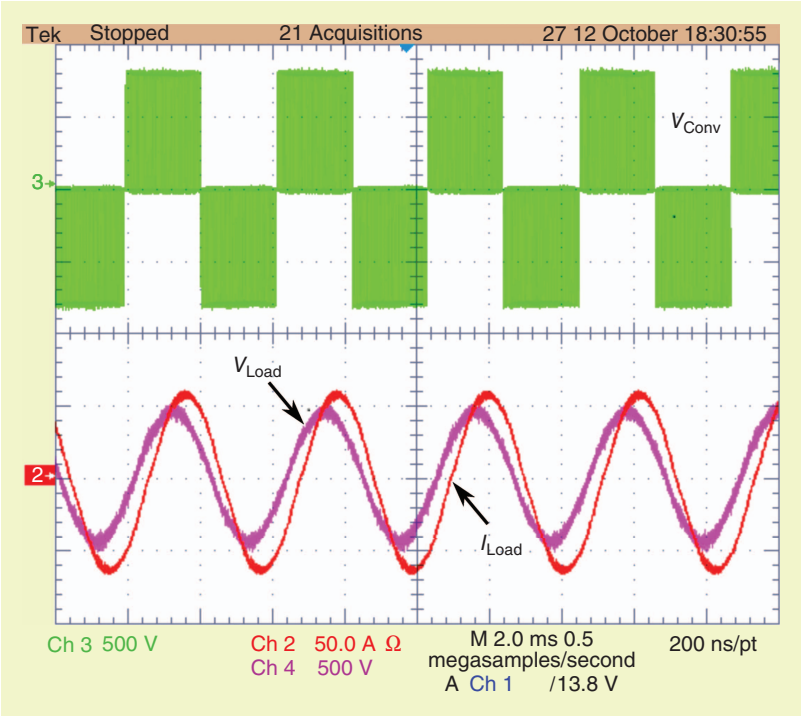

FIG 12 Experimental waveforms of the 1,200-V SiC MOSFET-based converter operating at 35 kVA. (Line current, I_{load}: 50 A/div; converter line voltage, V_{conv}: 500 V/div; load line voltage, V_{load}: 500 V/div; time: 2 ms/div.)

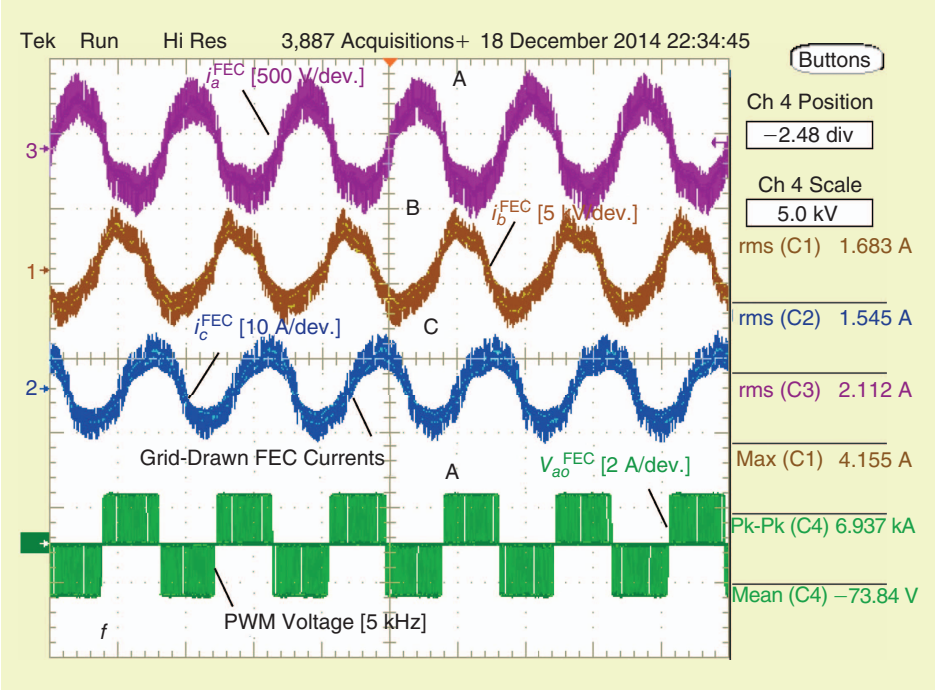

FIG 13 The AFEC converter three-phase currents and phase A pole voltage under ac 3.42-kV grid-tied TIPS system integration mode.

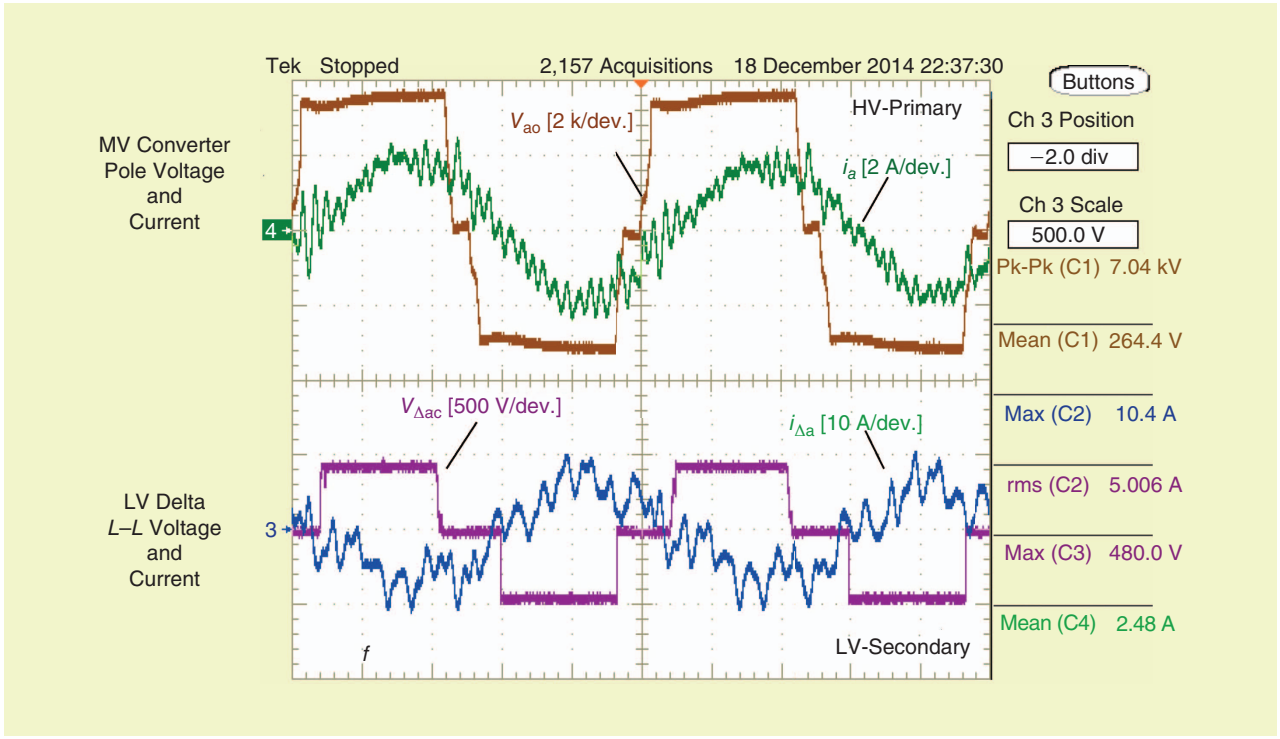

FIG 14 DABC operation results under TIPS system integration mode at 7-kV–420-V dc voltages at 8.4-kW and 10-kHz switching frequency.

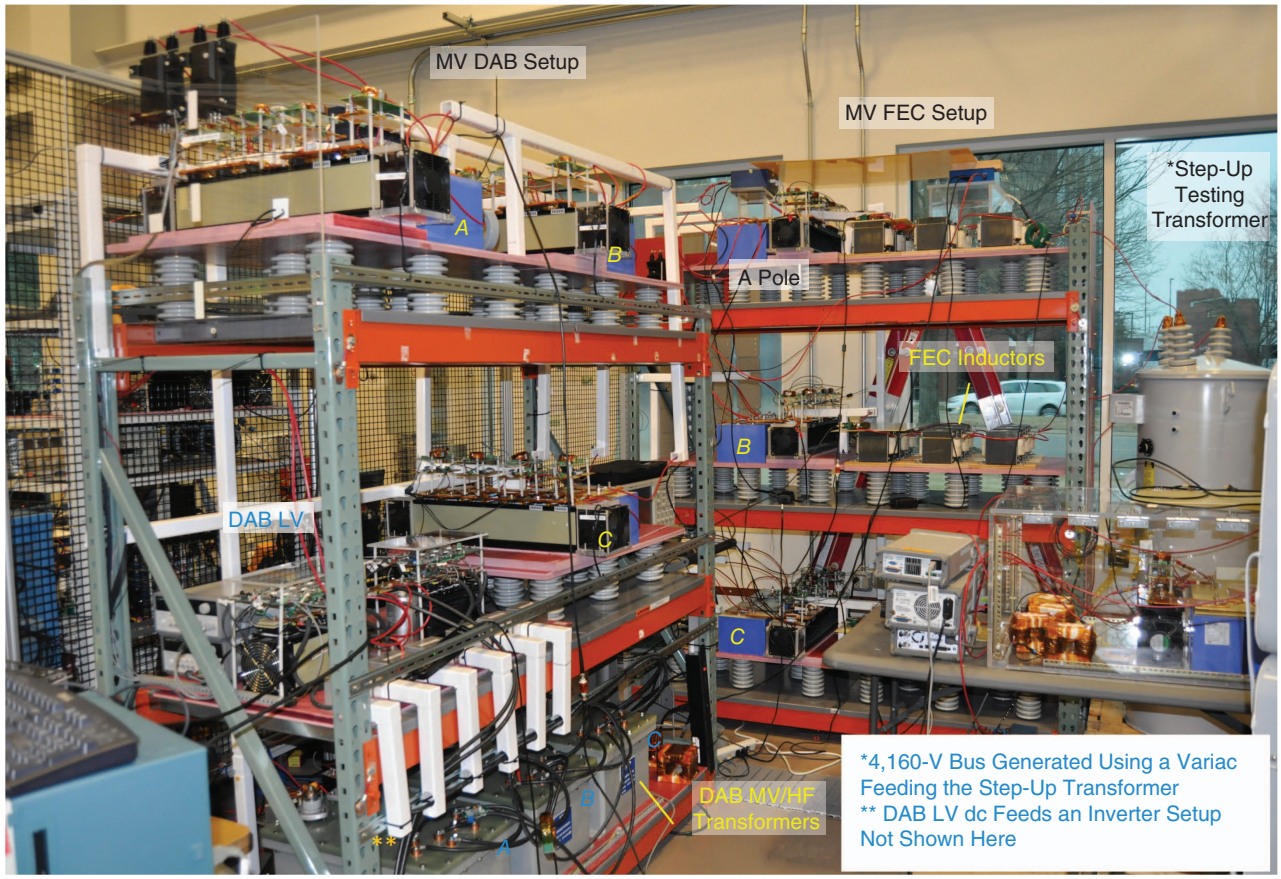

FIG 15 The TIPS system experimental setup at the NCSU FREEDM Systems Center laboratory.

Table 1. TIPS AFEC loss distribution at 3-kHz, 100-kVa, 13.8-kV grid at 22-kV dc bus.

Loss Component	UPF Mode	STATCOM Mode
Total switching loss (W)	440	370
Total conduction loss (W)	102	79.5
Total loss (W)	542	449.5
Efficiency (%)	99.46	99.55

Table 2. TIPS DABC loss distribution at 10 kHz, 100 kVA at 22-kV dc bus to 800-V dc bus operation.

Loss Component	Value
MV-side switching loss (W)	601. 86
MV-side conduction loss (W)	84.06
LV-side switching loss (W)	86.34
LV-side conduction loss (W)	511.05
HF transformer loss (W)	390
Total loss (W)	1,673.31
Efficiency (%)	98.33

Table 3. TIPS LV converter loss distribution at 20-kHz, 100-kVA, and 800-V dc bus.

Loss Component	UPF	STATCOM
One converter switching loss (W)	99	105
One converter conduction loss (W)	246	197
One converter total loss (W)	345	302
Total loss for three converters (W)	1035	906
Efficiency (%)	98.97	99.04

Table 4. TIPS overall loss distribution.

Loss Component	FEC (UPF)	DABC	LV Side (UPF)	Total Loss
Switching loss (W)	440	688.2	297	1,425.2
Conduction loss (W)	102	595.1	738	1,435.1
HF transformer loss (W)		390		390
Total loss (W)	542	1,673.3	1,035	3,250.3
Efficiency (%)	99.46	98.33	98.97	96.75

Figure 15 shows the TIPS system experimental test setup in the laboratory.

TIPS Loss Analysis

The power loss in each of the three stages of the TIPS is calculated from Piecewise Linear Electrical Circuit Simulation thermal simulations based on experimentally measured loss data of the 15-kV SiC IGBT, 1,200 V SiC MOSFET, and HF transformer. The loss is calculated for a 100-kVA TIPS system. Tables 1–3 summarize this loss information for each stage. The total loss of the TIPS is given in Table 4. The reverse recovery loss of the 10-kV SiC JBS diode is assumed to be negligible.

Conclusions

The foremost advantage of the 15-kV SiC IGBT is that it enables simplified converter topologies for MV applications. This feature is exploited by the proposed three-phase all-SiC SST, the TIPS system, with a simple three-level topology for 13.8-kV MV grid interface. This article highlights the characteristics of the 15-kV SiC IGBT, MV isolated gate driver, AFEC, DABC, LV converters, and their associated controls for TIPS system demonstration. The multistage modular structure of the TIPS system enabled the testing of individual phases up to 10 kV, 7.5 kW before integrating them into the overall closed-loop system. The MV gate driver was evaluated up to 11 kV, with dv/dt of over 100 kV/μs to handle the high-stress conditions imposed by fast switching 15-kV SiC IGBTs. The design issues of the *LCL* filter for the MV grid-tied AFEC as well as the control techniques for multistage converter integration are presented. The importance of low-capacitance design of the isolation HF transformers in DABC is emphasized based on the MV experimental results.

The design methods and considerations presented in this article serve as guidelines for development of MV SiC-based power-conversion systems, which have the potential to play a vital role in next-generation distribution power systems control and operation, MV motor drives for many applications, and MV grid-tied converters for renewable energy integration.

At this time, the 15-kV SiC IGBT used in the TIPS system is experimental and not commercially available. With future commercialization of HV SiC devices, more industries focusing on grid-connected power electronics will develop commercial SSTs applied to distributed renewable energy integration, MV motor drives, MV traction applications, MV shipboard power systems, disaster-recovery transformers, and many other applications.

About the Authors

Krishna Mainali (kmainal@ncsu.edu) received his B.E. degree in electrical and electronics engineering from the National Institute of Technology, Karnataka, India, in 2002 and his M.Eng. and Ph.D. degrees from the Department of Electrical and Computer Engineering, National University of Singapore (NUS) in 2005 and 2011, respectively. From 2008 to 2011, he was a member of the teaching staff at NUS. From 2011 to 2013, he worked as a research scientist at the Institute of Microelectronics, A*STAR, Singapore. His current research interests include electromagnetic compatibility in power electronics, solid-state transformers, and renewable energy applications. He is currently working as a postdoctorate researcher at the Future Renewable Electrical Energy Delivery and Management Systems Center, North Carolina State University, Raleigh.

Awneesh Tripathi (aktripat@ncsu.edu) earned his B.Tech. degree in electrical engineering from Harcourt Butler Technological Institute, Kanpur, India, in 2006 and his M.E. degree in electrical engineering from the Indian Institute of Science, Bangalore, India, in 2008. He worked at

S.M. Creative Electronics Ltd., Gurgaon, India, from 2008 to 2009 as a design engineer for dc–dc converters. He briefly taught at ITM, Gurgaon, prior to joining North Carolina State University (NCSU) in 2011 as a Ph.D. student. His research interests include high-power, medium-voltage dc–dc converter topologies; field-programmable gate array and digital signal processing-based control; electrical drives; and grid interfaces for renewable energy sources. He is currently working toward his Ph.D. degree at the Future Renewable Electrical Energy Delivery and Management Systems Center, NCSU, Raleigh.

Sachin Madhusoodhanan (sachin@ncsu.edu) received his B.Tech. degree in electrical and electronics engineering from the National Institute of Technology, Calicut, India, in 2007 and his M.E. degree in electrical engineering from the Indian Institute of Science, Bangalore, India, in 2009. From 2009 to 2011, he was with Ashok Leyland Limited, Chennai, India, as a senior engineer in the Advanced Engineering Department. In August 2011, he joined the U.S. National Science Foundation Future Renewable Electrical Energy Delivery and Management Systems Center at North Carolina State University, Raleigh, as a Ph.D. scholar. His research interests include power electronics, medium-voltage high-power converters, wide-bandgap power device applications, solid-state transformers, motor drives, and renewable energy integration.

Arun Kadavelugu (akkadave@ncsu.edu) received his B.E. degree in electrical engineering from Osmania University, Hyderabad, India, in 2005; his M.Tech. degree in power electronics from the Indian Institute of Technology (IIT), Kanpur, India, in 2007; and his Ph.D. degree from North Carolina State University (NCSU), Raleigh, in 2014. Prior to his Ph.D. studies, he worked as a senior project associate at IIT, Kanpur, on implementing an off-grid renewable-energy-based power plant. He is currently with ABB Corporate Research, Raleigh, North Carolina. He has worked on gate driver development for 15-kV SiC IGBTs, characterizing 10-kV SiC MOSFETs and 15-kV SiC IGBTs, and two- and three-level converter design and demonstration using these devices.

Dhaval Patel (todhavalcpatel@gmail.com) received his B.E. degree in power electronics engineering from Saurashtra University, Rajkot, India, in 2002; his M.E. degree in electrical engineering with a specialization in power electronics and drives from Gujarat University, India, in 2004; and his Ph.D. degree from the Indian Institute of Technology Bombay, Mumbai, India, in 2012. He was a postdoctoral research fellow with Future Renewable Electrical Energy Delivery and Management Systems Center, North Carolina State University (NCSU), Raleigh, from 2012 to 2014. His research interests include modulation and control techniques for power converters and high-power-density converter design. He is currently with NCSU.

Samir Hazra (shazra@ncsu.edu) received his B.E. (honors) degree in power engineering from Jadavpur University, Kolkata, India, in 2005 and his M.Tech. degree in electrical engineering from the Indian Institute of Technology Kanpur, India, in 2008. From 2005 to 2006, he was with SIEMENS, Kolkata, India, and from 2008 to 2011, he was with TVS Motors Company Ltd., Hosur, India, working as a power electronics and control engineer. His research interests include the solid-state transformers, wide-bandgap power-device-based medium-voltage power conversion, motor drives, and renewable energy integration. He is currently working toward his Ph.D. degree at the U.S. National Science Foundation Future Renewable Electrical Energy Delivery and Management Systems Center, North Carolina State University, Raleigh.

Kamalesh Hatua (kamalesh@ee.iitm.ac.in) received his B.E. degree in electrical and electronics engineering from Karnataka Regional Engineering College, Surathkal, India, in 2000, and his M.S. and Ph.D. degrees in electrical engineering from the Indian Institute of Science, Bangalore, India, in 2004 and 2011, respectively. He was with Bharat Earth Movers Ltd., Mysore, India, from 2000 to 2001 and with Honeywell Technology Solutions Laboratory, Bangalore, from 2004 to 2005. He was a postdoctoral research fellow with the Future Renewable Electrical Energy Delivery and Management Systems Center, North Carolina State University, Raleigh. His research interests include medium-voltage electric drives, polyphase induction motor drives, solid-state transformers, the design of high-efficiency power converters using upcoming silicon carbide power switches, and digital signal processing and field-programmable gate array-based controller design for power electronic applications. He is currently an assistant professor in the Department of Electrical Engineering, Indian Institute of Technology Madras, Chennai, India.

Subhashish Bhattacharya (sbhatta4@ncsu.edu) received his B.E. (honors) degree in electrical engineering from the Indian Institute of Technology, Roorkee, India, in 1986; his M.E. degree in electrical engineering from the Indian Institute of Science Bangalore, India, in 1988; and his Ph.D. degree in electrical engineering from the University of Wisconsin–Madison in 2003. He worked in the Flexible Alternating Current Transmission System (FACTS) and Power Quality Group at Westinghouse (later part of Siemens Power T&D) from 1998 to 2005. He joined North Carolina State University, Raleigh, as an assistant professor in August 2005, where he is currently the ABB term professor and a faculty member of the U.S. National Science Foundation Future Renewable Electrical Energy Delivery and Management Systems Center, Advanced Transportation Energy Center, and Department of Energy National Network for Manufacturing Innovation Power America. His research interests include solid-state transformers, wide-bandgap device-based medium-voltage power-conversion systems, high-frequency magnetics, and FACTS applications.

References

[1] J. Wang, A. Q. Huang, W. Sung, Y. Liu, and B. J. Baliga, "Smart grid technologies: development of 15-kV SiC IGBTs and their impact on utility applications," *IEEE Ind. Electron. Mag.*, vol. 3, no. 2, pp. 16–23, June 2009.

[2] K. Motto, Y. Li, and A. Q. Huang, "Comparison of the state-of-the-art high power IGBTs, GCTs and ETOs," in *Proc. IEEE Applied Power Electronics Conf. Expo.*, 2000, vol. 2, pp. 1129–1136.

[3] A. Agarwal, M. Das, B. Hull, S. Krishnaswami, J. W. Palmour, J. Richmond, S. Ryu, and J. Zhang, "Progress in silicon carbide power devices," in *Proc. Device Research Conf.*, 2006, pp. 155–158.

[4] D. Aggeler, J. Biela, and J. W. Kolar, "Solid-state transformer based on sic jfets for future energy distribution systems," in *Smart Energy Strategies: Meeting the Climate Change Challenge*. Zurich, Switzerland: vdf Hochschulverlag AG an der ETH Zurich, 2008, pp. 29–32.

[5] J. W. Palmour, L. Cheng, V. Pala, E. V. Brunt, D. J. Lichtenwalner, G.-Y. Wang, J. Richmond, M. O'Loughlin, S. Ryu, S. T. Allen, A. A. Burk, and C. Scozzie, "Silicon carbide power MOSFETs: Breakthrough performance from 900 V up to 15 kV," in *Proc. IEEE Int. Symp. Power Semiconductor Devices ICs*, 2014, pp. 79–82.

[6] S. Ryu, C. Capell, C. Jonas, Y. Lemma, M. O'Loughlin, J. Clayton, E. van Brunt, K. Lam, J. Richmond, A. Burk, D. Grider, S. Allen, J. Palmour, A. Agarwal, A. Kadavelugu, and S. Bhattacharya, "Ultra high voltage IGBTs in 4H-SiC," in *Proc. IEEE Workshop Wide Bandgap Power Devices Applications*, 2013, pp. 36–39.

[7] M. K. Das, C. Capell, D. E. Grider, R. Raju, M. Schutten, J. Nasadoski, S. Leslie, J. Ostop, and A. Hefner, "10 kV, 120 A SiC half H-bridge power MOSFET modules suitable for high frequency, medium voltage applications," in *Proc. Energy Conversion Congr. Expo.*, 2011, pp. 2689–2692.

[8] F. Wang, G. Wang, A. Huang, W. Yu, and X. Ni, "Design and operation of a 3.6 kV high performance solid state transformer based on 13 kV SiC MOSFET and JBS diode," in *Proc. IEEE Energy Conversion Congr. Expo.*, 2014, pp. 4553–4560.

[9] K. Hatua, S. Dutta, A. Tripathi, S. Baek, G. Karimi, and S. Bhattacharya, "Transformer less Intelligent power substation design with 15kV SiC IGBT for grid interconnection," in *Proc. IEEE Energy Conversion Congr. Expo.*, 2011, pp. 4225–4232.

[10] R. W. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft-switched high-power-density dc/dc converter for high-power applications," *IEEE Trans. Ind. Applicat.*, vol. 27, no. 1, pp. 63–73, 1991.

[11] A. Kadavelugu, S. Bhattacharya, S. Ryu, E. V. Brunt, D. Grider, and S. Leslie, "Experimental switching frequency limits of 15 kV SiC N-IGBT module," in *Proc. IEEE International Power Electronics Conf.*, 2014, pp. 3726–3733.

[12] A. Kadavelugu, S. Bhattacharya, S.-H. Ryu, E. van Brunt, D. Grider, A. Agarwal, and S. Leslie, "Characterization of 15 kV SiC n-IGBT and its application considerations for high power converters," in *Proc. IEEE Energy Conversion Congr. Expo.*, 2013, pp. 2528–2535.

[13] A. Kadavelugu, S. Bhattacharya, S. Ryu, D. Grider, S. Leslie, and K. Hatua, "Understanding dv/dt of 15 kV SiC N-IGBT and its control using active gate driver," in *Proc. IEEE Energy Conversion Congr. Expo.*, 2014, pp. 2213–2220.

[14] (2015, July 19). [Online]. Available: https://igbt-driver.power.com/products/scale-2-dc-dc-converters/iso3116i/iso3116i-65/

[15] A. Kadavelugu and S. Bhattacharya, "Design considerations and development of gate driver for 15 kV SiC IGBT," in *Proc. IEEE Applied Power Electronics Conf. Expo.*, 2014, pp. 1497–1501.

[16] A. Kadavelugu, K. Mainali, D. Patel, S. Madhusoodhanan, A. Tripathi, K. Hatua, S. Bhattacharya, S.-H. Ryu, D. Grider, and S. Leslie, "Medium voltage power converter design and demonstration using 15 kV SiC N-IGBTs," in *Proc. IEEE Applied Power Electronics Conf. Expo.*, 2015, pp. 1396–1403.

[17] S. Madhusoodhanan, A. Tripathi, D. Patel, K. Mainali, A. Kadavelugu, S. Hazra, S. Bhattacharya, and K. Hatua, "Solid state transformer and MV grid tie applications enabled by 15 kV SiC IGBTs and 10 kV SiC MOSFETs based multilevel converters," *IEEE Trans Ind. Applicat.*, vol. 51, no. 4, pp. 3343–3360, July–Aug. 2015.

[18] B. Wu, *High-power converters and AC Drives*. Hoboken, NJ: Wiley, 2006.

[19] S. Madhusoodhanan, K. Hatua, and S. Bhattacharya, "A unified control scheme for harmonic elimination in the front end converter of a 13.8 kV, 100 kVA transformerless intelligent power substation grid tied with LCL filter," in *Proc. IEEE Applied Power Electronics Conf. Expo.*, 2014, pp. 964–971.

[20] K. Mainali, S. Madhusoodhanan, A. Tripathi, D. Patel, S. Bhattacharya, "Start-up scheme for solid state transformers connected to medium voltage grids," in *Proc. IEEE Applied Power Electronics Conf. Expo.*, 2015, pp. 1014–1021.

[21] A. Tripathi, K. Mainali, D. Patel, A. Kadavelugu, S. Hazra, S. Bhattacharya, and K. Hatua, "Design considerations of a 15kv SiC IGBT enabled high-frequency isolated dc-dc converter," *IEEE Trans. Ind. Applicat.*, vol. 51, no. 4, pp. 3284–3294, July–Aug. 2015.

[22] G. Ortiz, M. Leibl, J. W. Kolar, and O. Apeldoorn, "Medium frequency transformers for solid-state-transformer applications—Design and experimental verification," in *Proc. IEEE Power Electronics Drive Systems Conf.*, 2013, pp. 1285–1290.

[23] L. Heinemann, "An actively cooled high power, high frequency transformer with high insulation capability," in *Proc. IEEE Applied Power Electronics Conf. Expo.*, 2002, pp. 352–357.

[24] K. Mainali, A. Tripathi, D. C. Patel, S. Bhattacharya, and T. Challita, "Design, measurement and equivalent circuit synthesis of high power HF transformer for three-phase composite dual active bridge topology," in *Proc. IEEE Applied Power Electronics Conf. Expo.*, 2014, pp. 342–349.

[25] S. P. Engel, N. Soltau, H. Stagge, and R. W. de Doncker, "Dynamic and balanced control of three-phase high-power dual-active bridge dc–dc converters in dc-grid applications," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1880–1889, 2013.

[26] A. Tripathi, M. Shah, S. Madhusoodhanan, S. Bhattacharya, and K. Hatua, "FPGA based control board development for medium-voltage high-power three-phase dual active bridge converter," in *Proc. IEEE 40th Annu. Conf. Industrial Electronics Society*, 2014, pp. 1487–1493.

[27] (2015, July 19). [Online]. Available: http://www.mskennedy.com/products/Bridges/MSK4804.prod

[28] S. Hazra, S. Madhusoodhanan, S. Bhattacharya, G. K. Moghaddam, and K. Hatua, "Design considerations and performance evaluation of 1200 V, 100 A SiC MOSFET based converter for high power density application," *IEEE Ind. Applicat. Mag.*, to be published.

[29] S. Madhusoodhanan, A. Tripathi, D. Patel, K. Mainali, and S. Bhattacharya, "Stability analysis of the high voltage dc link between the FEC and dc-dc stage of a transformer-less intelligent power substation," in *Proc. IEEE Energy Conversion Congr. Expo.*, 2014, pp. 3702–3709.

[30] S. Madhusoodhanan, A. Tripathi, A. Kadavelugu, S. Hazra, D. Patel, K. Mainali, K. Hatua, and S. Bhattacharya, "Experimental validation of the steady state and transient behavior of a transformer-less intelligent power substation," in *Proc. IEEE Applied Power Electronics Conf. Expo.*, 2014, pp. 3477–3484.

[31] S. Madhusoodhanan, K. Mainali, A. Tripathi, A. Kadavelugu, D. Patel, and S. Bhattacharya, "Thermal design considerations for medium voltage power converters with 15 kV SiC IGBTs," in *Proc. IEEE Int. Symp. Power Electronics for Distributed Generation Systems*, Aachen, Germany, June 2015.

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