Distributed Control and Redundant Technique to Achieve Superior Reliability for Fully Modular Input-Series-Output-Parallel Inverter System

Tianzhi Fang, *Member, IEEE*, Le Shen, Wei He, and Xinbo Ruan, *Fellow, IEEE*

***Abstract*—Input-series-output-parallel (ISOP) inverter system is very suitable for high input voltage and large output current power conversion applications. One of many merits of this assembly system lies in that its characteristic of multimodule series–parallel combination can significantly improve the reliability of the operation. To address this point, redundancy should be realized for the whole system. However, the existing methods for the ISOP inverter system all belong to centralized control, which restricts the modularity of the system. From the above perspective, this paper proposes a new scheme to achieve both power balance and distributed configuration according to the conception of compound control. Also, the relationship of control loops is analyzed and the design procedure of them is given. Based on the fully modular system actualized by the distributed control, the hot-swap technique is then raised to get a redundant system with superior reliability. Here, the way of bypassing other than cutting off is adopted to fulfill withdrawal of the faulty module from the system due to series connection at the input terminal. In addition, the detailed timing sequence of system operation is provided to ensure the smooth transition during the hot-plugging transient. Finally, a three-module prototype is built and the experimental results validate the effectiveness of the presented strategy.**

***Index Terms*—Bypass, distributed, inverter, input-series-output-parallel, redundancy.**

I. Introduction

As a crucial branch of system integration, series–parallel power conversion system combined with building block modules has been a hot research point in the field of power electronics at present. To meet the diverse application requirements at input or output terminals of power supply, multiple standardized converter modules can comprise four kinds of series–parallel combined systems, which are input-parallel-output-parallel (IPOP), input-parallel-output-series (IPOS), input-series-output-parallel (ISOP), and input-series-output-series (ISOS) [1], [2]. In the meanwhile, the basic constituent module could be dc–dc converter, dc–ac inverter, ac–dc rectifier, and ac–ac converter. Compared with the control of the dc–dc converter series–parallel systems [3]–[7], the regulation of the combined systems with the dc–ac inverter as the elementary cell is much more complicated since more variables such as the amplitude, phase, and frequency of modular ac output voltage (OV) or current have to be adjusted to ensure power balance of the whole system.

For the IPOP inverter system, the one with much more mature research of four inverter series–parallel combined systems, wide and deep explorations have been developed to form a systematic research theory over the years [8]–[24]. Its existing control strategy has experienced the evolution from centralized control [9], master-slave control [10], [11] to distributed control, which basically consists of two categories, i.e., the instantaneous current control [12]–[16] and the wireless droop technique [17]–[21]. All of these control methods achieve power balance by equalizing the ac output current of each module because the parallel input voltages are naturally equivalent and the control of output currents can guarantee the stable operation of the system. Moreover, the redundant operation has been realized on the basis of the distributed control for the IPOP inverter system [22]–[24]. Actually, the realization of redundancy function is another significant objective for series–parallel systems except for the achievement of power balance since it can improve the reliability of the whole system.

Input-series inverter system, including the ISOP and ISOS inverter system, is quite suitable for high input voltage applications such as the ship-electric-power-distribution systems, high-speed railway electrical systems, etc. [25]–[27]. Since the modules of the system are connected in series at the input sides, voltage stress of the switching devices is reduced and more appropriate devices can be chosen. For ISOS inverter system, a control strategy, which combines an input voltage sharing (IVS) control with synchronization of the output phase angles, is proposed to achieve IVS and OVS simultaneously [28]. Moreover, a cross-feedback output-voltage control scheme is put forward to realize the power balance [29]. In this scheme, individual modulation signals are obtained by multiplying the common OV loop output with its respective magnitude compensation loop output. Like the ISOS inverter system, the cascaded multilevel inverter [30]–[32] also provides a good solution for the high voltage ac output occasion. While, a larger number of levels increase the control complexity, and full modularity and redundancy is relatively slightly difficult to carry out compared with the series–parallel system. Meanwhile, the ISOP inverter system could be even applied to large current ac output occasions. Obviously this composition could also enhance the system credibility as

Manuscript received October 8, 2015; revised January 6, 2016; accepted February 1, 2016. Date of publication February 16, 2016; date of current version September 16, 2016. This work was supported by the National Natural Science Foundation of China under Award 51477076 and the Natural Science Foundation of Jiangsu Province under Award BK20131363. Recommended for publication by Associate Editor G. Moschopoulos.

The authors are with the Center for More-Electric-Aircraft Power System, College of Automation Engineering, Nanjing University of Aeronautics and Astronautics, Nanjing 210016, China (e-mail: fangtianzhi@126.com; shenle0517@126.com; heweinuaa@126.com; ruanxb@nuaa.edu.cn).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2016.2530809

well as other series–parallel combined systems containing the IPOP inverter system. But unlike the developed IPOP inverter system, the research on the ISOP inverter system is just at the primary stage. As for this system, it is pointed out that the output current sharing (OCS) control with direct feedback of each module's own output inductor current will lead to the unstable system, and then a three-loop control strategy is put forward to achieve IVS and OCS [33], [34]. Further, based on the method, an improved solution is raised to expedite the regulation speed [35]. Both of two methods have the common OV control loop. Additionally, a cross-feedback output-inductor-current-sharing control scheme is brought up to reach the goal of energy equilibrium effectively for the ISOP high-frequency ac link inverters [36]. Similarly, the tactic possesses the common OV regulation loop. And what's more, the current feedback for every individual inner current loop is the sum of other output inductor currents instead of its own. So all the modules are inevitably mutual coupling, which restricts the modularity of the ISOP inverter system. In brief, all of the aforementioned control strategies give the concrete measures on how to earn power balance among modules in the system. Nevertheless, they are actually centralized control and the system tends to collapse if the central control unit or common control loop goes wrong. So the distributed control and modularity have not been accomplished yet for the ISOP inverter system, and the control methods now available are far from the target of redundancy. That is to say, we cannot practically heighten the dependability by the foregoing control alternatives. Therefore, the way to attain the distributed and redundant control is urgently needed to be offered.

To achieve fault tolerance of the ISOP inverter system indeed, two steps have to be executed with power sharing realized simultaneously just like the IPOP inverter system. The first is to fulfill the distributed control, i.e., to scatter all the control units into each module. The second is to actualize the hot swap for the sake of boosting the reliability of the whole system. In the light of the idea, this paper is organized as follows. It starts with the conception of compound control to acquire the power balance of the ISOP inverter system. Then, an implemental control method and a novel distributed architecture are proposed. As regard to the distributed control scheme, the relationship of control loops is analyzed and design procedure of them is given out successively. Based on the distributed control, the redundant technique is introduced. Here, to realize the exit of the faulty module, we particularly employ the way of bypassing, which is quite different from the redundancy scheme for the IPOP inverter system. Also the timing sequence of hot plugging is provided. Last, a three-module prototype is built and the experimental results validate the effectiveness of the above strategy.

II. Control Conception to Achieve Power Balance

For ISOP inverter system, one of two objectives is to achieve power balance. So, here, we shall study the control idea on how to reach the goal first. Fig. 1 gives the schematic block of the ISOP inverter system consisting of n modules, where $C_{d1}, C_{d2}, \ldots, C_{dn}$ are the input dividing capacitors. Besides, $S_{11}, S_{21}, \ldots, S_{n1}$ are input relays and $R_1, R_2, \ldots, R_n$ are the

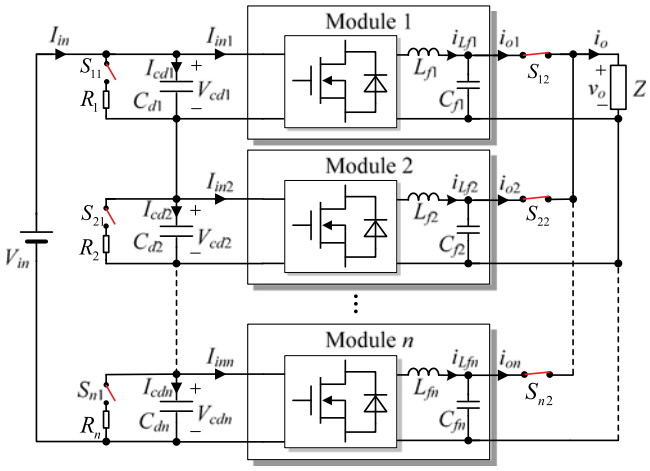


Fig. 1. Schematic block of n-module ISOP inverter system.

current limiting resistances. While, $S_{12}, S_{22}, \ldots, S_{n2}$ are output relays. Here S_{j1}, R_j and $S_{j2} (j = 1, 2, \ldots, n)$ are applied to the operation of redundancy for ISOP inverter system and their detailed function will be illustrated in Section IV.

From Fig. 1, we can even find modular input voltages and input currents as $V_{cd1}, V_{cd2}, \ldots, V_{cdn}$, and $I_{\mathrm{in}1}, I_{\mathrm{in}1}, \ldots, I_{\mathrm{in}n}$, respectively. Also, modular output inductor currents and output currents as $i_{Lf1}, i_{Lf2}, \ldots, i_{Lfn}$ and $i_{o1}, i_{o2}, \ldots, i_{\mathrm{on}}$ are shown separately. Suppose the efficiency of each module is 100%. Then, by power conservation, we have

$$\begin{aligned} P_{\mathrm{in}j} &= V_{cdj} \cdot I_{\mathrm{in}j} = V_o \cdot I_{oj} \cdot \cos\theta_j \\ &= V_o \cdot I_{Lfj} \cdot \cos\varphi_j = P_{oj}, \quad j = 1, 2, \ldots, n \end{aligned} \tag{1}$$

where $P_{\mathrm{in}j}, P_{oj}$ are modular input power and output active power. I_{oj}, I_{Lfj}, and V_o are rms values of modular output currents, output inductor currents, and system OV, respectively. θ_j, φ_j are separately power factor angles and phase angles between output inductor currents and OV.

We know that OCS means the power balance at the output terminal which involves the current stress balance in the power devices of each module. While it is output filter inductor current i_{Lfj} but not i_{oj} that flows through the switches. So, here, OCS refers to output inductor current sharing since the currents in power devices of the modules are balanced if the output inductor currents are balanced.

For input-series-connected inverter systems (including ISOP inverter system), the control at the output terminal (namely OCS control with direct feedback of each module's own output inductor current) is not stable [28], [34]. On the other hand, if the control at the input terminal is adopted (namely IVS control), we have

$$V_{cd1} = V_{cd2} = \cdots = V_{cdn}. \tag{2}$$

At steady state, all the input dividing capacitor voltages are kept constant so that the average current of each input dividing capacitor is zero. Thus, we get

$$I_{\mathrm{in}1} = I_{\mathrm{in}2} = \cdots = I_{\mathrm{in}n}. \tag{3}$$

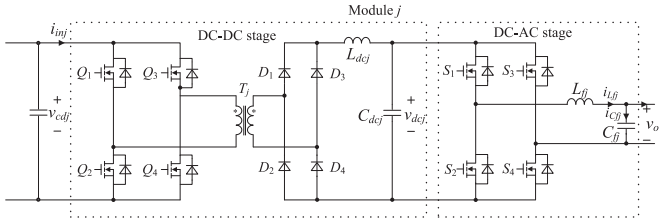


Fig. 2. Main circuit of the module.

Combine (1), (2), and (3), we have

$$V_o \cdot I_{Lf1} \cdot \cos\varphi_1 = V_o \cdot I_{Lf2} \cdot \cos\varphi_2 = \cdots = V_o \cdot I_{Lfn} \cdot \cos\varphi_n. \quad (4)$$

It can be seen that IVS control for ISOP inverter system only guarantees the balance of modular active power.

Furthermore, on the basis of IVS control (namely IVS is achieved) we could then go a step further by two means. On one hand, if we keep φ_j (phase angle between individual output inductor current and OV) the same, namely

$$\varphi_1 = \varphi_2 = \cdots = \varphi_n. \quad (5)$$

Combine (4) and (5), we have

$$I_{Lf1} = I_{Lf2} = \cdots = I_{Lfn}. \quad (6)$$

Accordingly, we can get

$$i_{Lf1} = i_{Lf2} = \cdots = i_{Lfn}. \quad (7)$$

Namely OCS can be achieved.

On the other hand, if IVS control is employed while keeping the amplitude of output inductor currents the same, namely (6) is satisfied, so is (5), thus (7) is obtained. Obviously, both of the two methods can achieve IVS and OCS. We refer to the control strategy that leads to power balance as compound control conception.

III. Distributed Scheme Based on Compound Control Conception

A. Selection of Modular Topology

Since modules of ISOP inverter system are connected in series at the input sides, isolated topologies should be adopted. As seen from Fig. 2 (where v_{cdj} refers to modular input voltage, namely the voltage of C_{dj}), each module employs a traditional two-stage structure: a phase-shifted full-bridge converter as the dc–dc stage followed by a full-bridge inverter as the dc–ac stage. Here the dc–dc stage is used for isolation and the high-frequency transformer introduced here could efficiently lower the volume of module. Obviously the two-stage approach is beneficial to modularity of the system.

B. Implementation of Compound Control and Distributed Configuration

Apart from power balance, the other objective for ISOP inverter system is to realize the redundancy so as to veritably enhance the reliability of the whole system. To attain the target, the first step we should do is to disperse all the control elements into each module, i.e., to acquire the distributed control.

As indicated in part II, ISOP inverter system can actualize power balance by ensuring the equivalency of the phase or amplitude of modular output inductor currents while controlling the input voltages the same. According to the first case of the compound control conception, Fig. 3 gives a specific implementation to achieve both power balance and distributed control. Here, IVS loop is employed to guarantee IVS of each module, and the multiplier is introduced to realize phase synchronization of modular output inductor current. So we can draw the conclusion that this method could bring about power sharing in the light of the preceding compound control idea and, therefore, it is entitled the way of IVS combined with the output inductor current phase synchronized.

Additionally, from the control configuration standpoint, all the modules have independent control loops and they correspond by buses in the scheme as seen in Fig. 3. Specifically, the two-loop control is adopted for single inverter. Its control loops contain the OV loop and the inner current loop which employs the hysteresis control. Meanwhile, for the whole system the two control loops mentioned above together with IVS loop are scattered into every inverter and they communicate with each other by three buses, including the IVS bus, the OV reference synchronous bus ($v_{\rm ref}$ synchronous bus) and the average current bus ($i_{\rm ave}$ bus). It's noteworthy that OV loop here is no longer communal for the whole system. In these separate OV loops, all the OV references are synchronized by digital signal processor (DSP) to create the $v_{\rm ref}$ synchronous bus. And, OVs of individual module are regulated by their respective OV loops. Since the components of feedback networks and regulators may have deviation, the output signals of every OV regulators (namely i_{gj}) are not exactly the same and so they are averaged as the common one to form the $i_{\rm ave}$ bus. The signal $i_{\rm ave}$ is then introduced into all inverter modules and served as the initial current reference. Furthermore, in the IVS loop, sampling signals of individual input voltages are connected through identical precise resistors to the same point to develop the IVS bus. The bus signal is then treated as input voltage reference $V_{\rm in\_ref}$, whose value can be easily got as $K_f \cdot V_{\rm in}/n$. Generated by input voltage regulator G_{vd}, the dc deviation signal $v_{{\rm dev}j}$, along with the initial current reference $i_{\rm ave}$ are sent to the constant-phase amplitude-shift unit, and its output signal $i_{{\rm ref}j}$ serves as the actual inductor current reference of respective modules.

Fig. 4(a) particularly gives the diagram of the constant-phase amplitude-shift unit, which is mainly composed of the multiplier. From the figure, we have

$$i_{{\rm ref}j} = i_{\rm ave} - i_{{\rm reg}j} = i_{\rm ave} - v_{{\rm dev}j} \cdot i_{\rm ave} \quad (8)$$

where $v_{{\rm dev}j}$ is a dc deviation and $i_{\rm ave}$ is a ac quantity. Simulation waveforms of the input and output signals of the multiplier are shown in Fig. 4(b). It can be seen that sinusoidal error signal $i_{{\rm reg}j}$ has the same phase angle with $i_{\rm ave}$ and its amplitude varies in accordance with $v_{{\rm dev}j}$. Further, the Fourier analysis of $v_{{\rm dev}j}$ and $i_{{\rm reg}j}$ are given out in Fig. 4(c), from which we can see that the frequency spectrum of the signal $i_{{\rm reg}j}$ is just the shift of the frequency spectrum of $v_{{\rm dev}j}$, that is, the frequency spectrum of

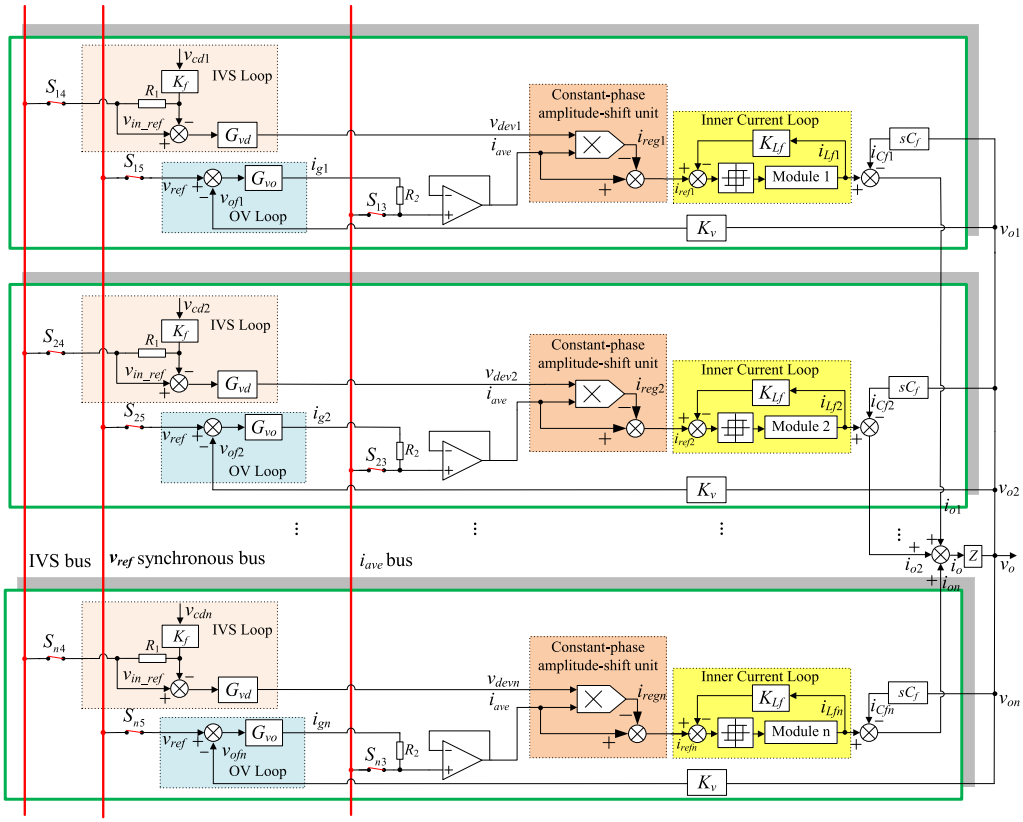


Fig. 3. Diagram of the distributed configuration and compound control strategy.

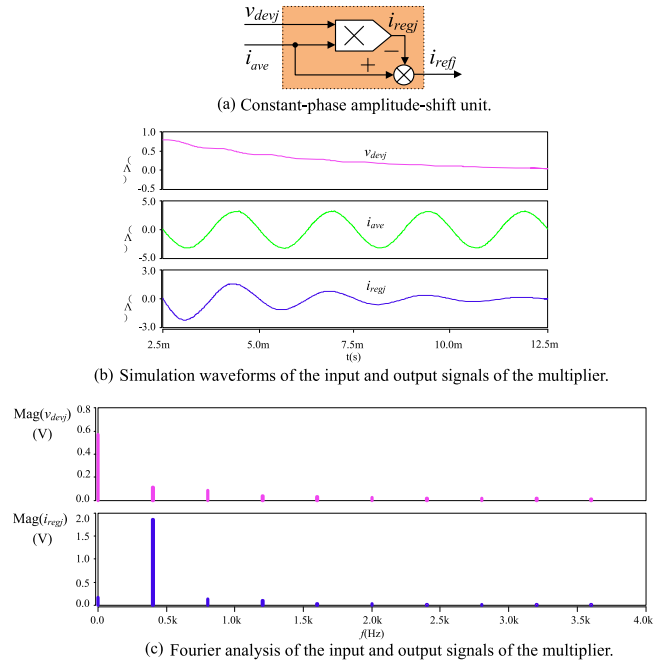
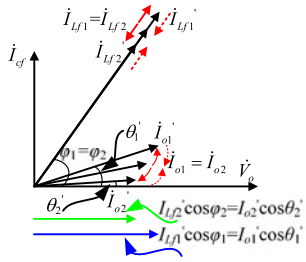


Fig. 4. Investigation on constant-phase amplitude-shift unit. (a) Constant-phase amplitude-shift unit. (b) Simulation waveforms of the input and output signals of the multiplier. (c) Fourier analysis of the input and output signals of the multiplier.

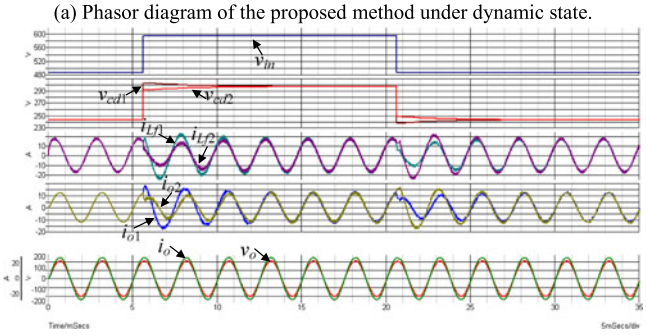
$v_{\mathrm{dev}j}$ is moved to the fundamental frequency 400 Hz to reach the frequency spectrum of $i_{\mathrm{reg}j}$. So $i_{\mathrm{reg}j}$ contains all the information of $v_{\mathrm{dev}j}$ and $v_{\mathrm{dev}j}$ actually adjusts the amplitude of i_{ave}.

Fig. 4(b) and (c) both prove that the IVS loop only adjusts the amplitude of the initial current reference i_{ave}. While, the phase angles of the initial current reference i_{ave}, the regulating quantity $i_{\mathrm{reg}j}$, and the actual inductor current reference $i_{\mathrm{ref}j}$ are kept the same. Accordingly, inductor currents (i_{Lfj}) of respective modules trace the same phase $i_{\mathrm{ref}j}$ to reach the phase synchronization, which is combined with the control of the IVS loop to achieve power balance. Specifically, the IVS loop adjusts the amplitude of the output inductor currents and, then, actually regulates the output real power to realize IVS of respective modules in the system. Simultaneously OCS of every module is also achieved according to the principle of the compound control mentioned earlier.

Without loss of generality, a two-module ISOP inverter system is taken as an example to elaborate the dynamic adjusting process of the proposed method with the illustration in Fig. 5. Suppose a perturbation occurs in the input voltage of module 1 and leads to the ascent of v_{cd1} and the descent of v_{cd2}, then, according to (8), we get $I_{\mathrm{ref}1} > I_{\mathrm{ave}} > I_{\mathrm{ref}2}$, namely the inductor current amplitude of module 1 is greater than that of module 2. The amplitude difference between i_{Lf1} and i_{Lf2} depends on $v_{\mathrm{dev}1}$ and $v_{\mathrm{dev}2}$. This will increase the active power of module 1 and decrease the active power of module 2. Finally, the system will return to balanced state and achieve IVS and OCS



(a) Phasor diagram of the proposed method under dynamic state.



(b) Simulation waveforms of the dynamic adjusting process.

Fig. 5. Dynamic adjusting process of the proposed method. (a) Phasor diagram of the proposed method under dynamic state. (b) Simulation waveforms of the dynamic adjusting process.

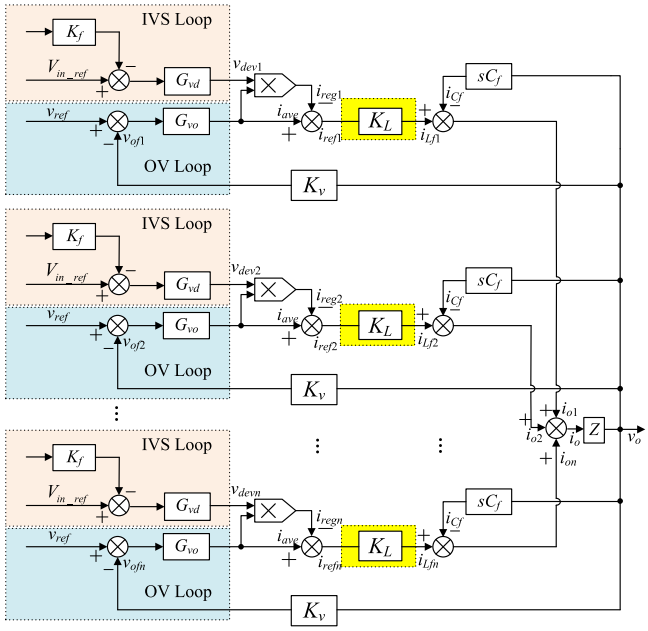
after several periods. Fig. 5(a) shows the phasor diagram of the control method under dynamic state. While, Fig. 5(b) gives the simulation waveforms of the system at nominal resistive load when input voltage steps up and down. Here, we intentionally make the two input dividing capacitors different. From the figure, we can see that the phase angles of output inductor currents are kept the same in the process of adjustment while the amplitude difference of output inductor current between the two modules diminishes as their input voltage difference declines. Characteristics of output inductor currents and output load currents are in accordance with previous analysis and phasor diagrams in Fig. 5(a).

C. Relationship of the Control Loops and Their Design

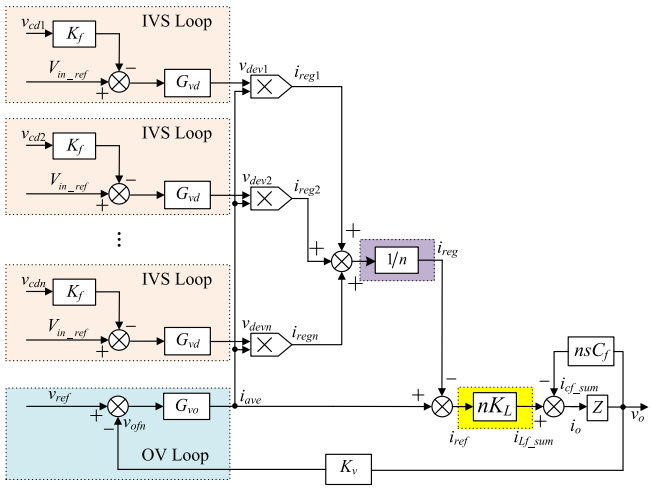
Due to the switching frequency of the inverter is much higher than the frequency of the OV, the inner current loop (see Fig. 3) which employs the hysteresis control can be seen as a proportional element [14], [15], which is denoted by K_L. Furthermore, from Fig. 3 we can get

$$\begin{aligned} i_{\text{ave}} &= \frac{1}{n}\cdot\sum_{j=1}^{n} i_{gj} = \frac{1}{n}\cdot\sum_{j=1}^{n} G_{vo}(v_{\text{ref}} - v_o\cdot K_v) \\ &= \frac{1}{n}\cdot G_{vo}\cdot[n\cdot(v_{\text{ref}} - v_o\cdot K_v)] = G_{vo}\cdot(v_{\text{ref}} - v_o\cdot K_v). \end{aligned} \tag{9}$$

So we can acquire Fig. 6(a), the equivalent control block diagram for distributed ISOP inverter system. From the figure, we can find that it is actually a multi-input multi-output control system. It seems that the control loops are mutual coupling, which will cause inconvenience for the loop design. So we have to analyze the relationship of them before conducting the design process.



(a) Equivalent control block diagram for distributed ISOP inverter system.



(b) Equivalent control block diagram for distributed ISOP inverter system.

Fig. 6. Equivalent control block diagram for distributed ISOP inverter system. (a) Equivalent control block diagram for distributed ISOP inverter system. (b) Simplified control block diagram.

From Fig. 6(a), we can get the expression of system output current as follows:

$$\begin{aligned} i_o &= \sum_{j=1}^{n} i_{oj}(s) = \sum_{j=1}^{n}\left(i_{Lfj}(s) - sC_f v_o\right) \\ &= \left[i_{\text{ave}}(s) - i_{\text{ave}}(s)\cdot\left(\sum_{j=1}^{n} v_{\text{dev}j}\right)\cdot\frac{1}{n}\right] \\ &\quad\cdot(nK_L) - nsC_f\cdot v_o. \end{aligned} \tag{10}$$

Hence, we can obtain the further simplified control block diagram as shown in Fig. 6(b). From the figure, we have

$$i_{\text{reg}j} = i_{\text{ave}}\cdot v_{\text{dev}j}. \tag{11}$$

Here, the small signal disturbances of input and OVs are denoted by $\hat{v}_{cdj}$ and $\hat{v}_o$. While the small signal disturbances of the output signals of IVS loops, OV loop and multipliers are denoted by $\hat{v}_{\mathrm{dev}j}$, $\hat{i}_{\mathrm{ave}}$, and $\hat{i}_{\mathrm{reg}j}$, respectively. So from (11), the small signal disturbance of $i_{\mathrm{reg}j}$ could be deduced as

$$\hat{i}_{\mathrm{reg}j} = V_{\mathrm{dev}j} \cdot \hat{i}_{\mathrm{ave}} + \hat{v}_{\mathrm{dev}j} \cdot I_{\mathrm{ave}} + \hat{v}_{\mathrm{dev}j} \cdot \hat{i}_{\mathrm{ave}}. \tag{12}$$

Since G_{vd} is realized by a proportional regulator [34], the steady value $V_{\mathrm{dev}j}$ equals to zero. After neglecting the second-order disturbance quantity, we have

$$\begin{aligned}\hat{i}_{\mathrm{reg}j} &= I_{\mathrm{ave}} \cdot \hat{v}_{\mathrm{dev}j} = I_{\mathrm{ave}} \cdot G_{vd} \cdot [V_{\mathrm{in\_ref}} - K_f \cdot (V_{cdj} + \hat{v}_{cdj})] \\ &= -K_f \cdot I_{\mathrm{ave}} \cdot G_{vd} \cdot \hat{v}_{cdj}. \end{aligned} \tag{13}$$

Then, we can further get

$$\hat{v}_{cdj} = \frac{-1}{K_f \cdot G_{vd} \cdot I_{\mathrm{ave}}} \cdot \hat{i}_{\mathrm{reg}j}. \tag{14}$$

Besides, from Fig. 6(b), we can derive

$$\begin{aligned}\hat{i}_{\mathrm{ref}} &= (\hat{i}_{\mathrm{ave}} - \hat{i}_{\mathrm{reg}}) = \hat{i}_{\mathrm{ave}} - \frac{1}{n} \cdot \sum_{j=1}^{n} \hat{i}_{\mathrm{reg}j} \\ &= \hat{i}_{\mathrm{ave}} - \frac{1}{n} \cdot \sum_{j=1}^{n} (-K_f \cdot I_{\mathrm{ave}} \cdot G_{vd} \cdot \hat{v}_{cdj}) \\ &= \hat{i}_{\mathrm{ave}} + \frac{1}{n} \cdot K_f \cdot I_{\mathrm{ave}} \cdot G_{vd} \cdot \sum_{j=1}^{n} \hat{v}_{cdj} \\ &= \hat{i}_{\mathrm{ave}} + 0 = \hat{i}_{\mathrm{ave}}. \end{aligned} \tag{15}$$

While

$$\hat{i}_{\mathrm{ave}} = -K_v \cdot G_{vo} \cdot \hat{v}_o. \tag{16}$$

So combine (15) and (16), we can acquire

$$\hat{v}_o = -\frac{1}{K_v \cdot G_{vo}} \cdot \hat{i}_{\mathrm{ref}}. \tag{17}$$

Here, we deem $\hat{v}_{cdj}$ and $\hat{v}_o$ as controlled variables of every control loop, and $\hat{i}_{\mathrm{reg}j}$ and $\hat{i}_{\mathrm{ref}}$ as control variables of corresponding loops. Then, combine (14) and (17), we can develop the following matrix equation: Equation (18) as shown at the bottom of the page.

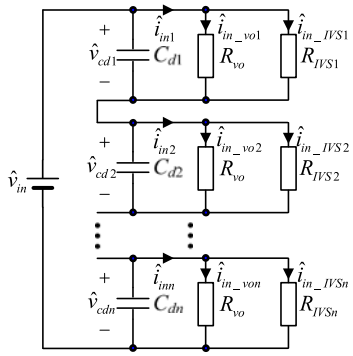


Fig. 7. Equivalent small signal model of ISOP inverter system with IVS control.

From the equation above, we can see that the n IVS loops and the system equivalent OV loop will not affect each other and so they are actually decoupled, which will be conducive for the control loop design. Consequently, we could carry out the design procedure of the IVS loop and the OV loop, respectively, as follows.

1) Design of IVSR: Based on the control strategy shown in Fig. 6(b), the load of each constituent inverter modules can be considered to be composed of two parts: one part is the *average system load*, which is determined by i_{ave}, the output of the OV loop; and the other part is the *dynamic load*, which is determined by $i_{\mathrm{reg}j}$ ($j = 1, 2, \ldots, n$), introduced by each IVS loops. So, at the input side of the inverter module, each inverter can be regarded as two resistances, the value of one resistance is determined by i_{ave}, and the value of the other resistance is determined by $i_{\mathrm{reg}j}$ ($j = 1, 2, \ldots, n$), as shown in Fig. 7.

If the IVS loops are removed (Seeing Fig. 3), i.e., $v_{\mathrm{dev}1} = v_{\mathrm{dev}2} = \ldots = v_{\mathrm{dev}n} = 0$, the method will be equivalent to OCS control with direct feedback of each module's own output inductor current, which will lead to an instable system since the modules take on the negative resistances at the input sides [34], so the resistance R_{vo} in Fig. 7 can be expressed as

$$\begin{aligned} R_{vo} &= -R_n = -\frac{(V_{\mathrm{in}}/n)^2}{P_o/n} \\ &= \frac{\hat{v}_{cdj}}{\hat{i}_{\mathrm{in\_}voj}}, \quad (j = 1, 2, \ldots, n) \end{aligned} \tag{19}$$

where P_o is system active output power.

$$\begin{bmatrix} \hat{v}_{cd1} \\ \hat{v}_{cd2} \\ \vdots \\ \hat{v}_{cdn} \\ \hat{v}_o \end{bmatrix} = \begin{bmatrix} \frac{-1}{K_f \cdot G_{vd} \cdot I_{\mathrm{ave}}} & 0 & \cdots & 0 & 0 \\ 0 & \frac{-1}{K_f \cdot G_{vd} \cdot I_{\mathrm{ave}}} & \ddots & 0 & 0 \\ \vdots & \ddots & \ddots & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{K_f \cdot G_{vd} \cdot I_{\mathrm{ave}}} & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{K_v \cdot G_{vo}} \end{bmatrix} \begin{bmatrix} \hat{i}_{\mathrm{reg}1} \\ \hat{i}_{\mathrm{reg}2} \\ \vdots \\ \hat{i}_{\mathrm{reg}n} \\ \hat{i}_{\mathrm{ref}} \end{bmatrix}. \tag{18}$$

From Fig. 6(b), the individual output current inductor perturbation $\hat{i}_{Lf\_\mathrm{IVS}j}$ ($j = 1, 2, \ldots, n$) introduced by the input voltage perturbation $\hat{v}_{cdj}$ ($j = 1, 2, \ldots, n$) can be expressed as

$$\hat{i}_{Lf\_\mathrm{IVS}j} = \hat{v}_{cdj} \cdot K_f \cdot G_{vd} \cdot i_{\mathrm{ave}}(s) \cdot K_L, (j = 1, 2, \ldots, n). \tag{20}$$

Please be noted that the individual $\hat{i}_{Lf\_\mathrm{IVS}j}$ ($j = 1, 2, \ldots, n$) has the same phase angle with individual i_{Lfj} ($j = 1, 2, \ldots, n$).

The perturbation on the system OV can be ignored because the OV of the ISOP inverter system is not affected by the IVS loops. Hence, the individual active output power perturbation $\hat{p}_{oj}$ ($j = 1, 2, \ldots, n$) can be expressed as

$$\hat{p}_{oj} = \hat{i}_{Lf\_\mathrm{IVS}j} \cdot V_o \cdot \cos\varphi_j, \quad (j = 1, 2, \ldots, n). \tag{21}$$

Assuming the conversion efficiency for each individual module is 100%, by power conservation, the input power perturbation equals to the output active power perturbation

$$\hat{p}_{\mathrm{in}j} = \hat{p}_{oj}, \quad (j = 1, 2, \ldots, n). \tag{22}$$

From Fig. 7, the module input power can be expressed as

$$\begin{aligned} \frac{P_{\mathrm{in}}}{n} + \hat{p}_{\mathrm{in}j} &= \left(\frac{V_{\mathrm{in}}}{n} + \hat{v}_{cdj}\right)(I_{\mathrm{in}} + \hat{i}_{\mathrm{in}j}) \\ &= \frac{V_{\mathrm{in}}}{n} \cdot I_{\mathrm{in}} + \hat{v}_{cdj} \cdot I_{\mathrm{in}} + \frac{V_{\mathrm{in}}}{n}(\hat{i}_{\mathrm{in\_IVS}j} + \hat{i}_{\mathrm{in}\_voj}) \\ &= \hat{v}_{cdj}(\hat{i}_{\mathrm{in\_IVS}j} + \hat{i}_{\mathrm{in}\_voj}), (j = 1, 2, \ldots, n). \end{aligned} \tag{23}$$

Neglecting the second-order term of (23) and noting that the dc terms on both sides of the equation are equal, we obtain

$$\begin{aligned} \hat{p}_{\mathrm{in}j} = {} & \hat{v}_{cdj} \cdot I_{\mathrm{in}} + \frac{V_{\mathrm{in}}}{n} \\ & \cdot (\hat{i}_{\mathrm{in\_IVS}j} + \hat{i}_{\mathrm{in}\_voj}), \quad (j = 1, 2, \ldots, n). \end{aligned} \tag{24}$$

From (20)–(22), and (24), we have

$$\begin{aligned} \hat{v}_{cdj} \cdot I_{\mathrm{in}} + \frac{V_{\mathrm{in}}}{n} \cdot (\hat{i}_{\mathrm{in\_IVS}j} + \hat{i}_{\mathrm{in}\_voj}) = \hat{v}_{cdj} \\ \cdot K_f \cdot G_{vd} \cdot i_{\mathrm{ave}}(s) \cdot K_L \cdot V_o \cdot \cos\varphi_j, \quad (j = 1, 2, \ldots, n). \end{aligned} \tag{25}$$

At the left-hand side of (25), the term $i_{\mathrm{ave}}(s) \cdot K_L$ equals to I_o/n, so $i_{\mathrm{ave}}(s) \cdot K_L \cdot V_o \cdot \cos\varphi_j$ equals to P_o/n. Combining with (19), (25) can be rewritten as

$$\frac{\hat{v}_{cdj}}{\hat{i}_{\mathrm{in\_IVS}j}} = \frac{V_{\mathrm{in}}}{K_f \cdot G_{vd} \cdot P_o} \triangleq R_{\mathrm{IVS}j}, \quad (j = 1, 2, \ldots, n). \tag{26}$$

Equation (26) implies that the role of IVS loops is equivalent to introduce a *positive resistance* to the input terminal of each module, which is in paralleled with the negative resistance. So, the equivalent input impedance of each inverter module is

$$\begin{aligned} Z_{\mathrm{in}} = {} & R_{vo} // R_{\mathrm{IVS}j} = \frac{-R_n \cdot R_{\mathrm{IVS}j}}{-R_n + R_{\mathrm{IVS}j}} \\ = {} & \frac{R_n \cdot R_{\mathrm{IVS}j}}{R_n - R_{\mathrm{IVS}j}}, \quad (j = 1, 2, \ldots, n). \end{aligned} \tag{27}$$

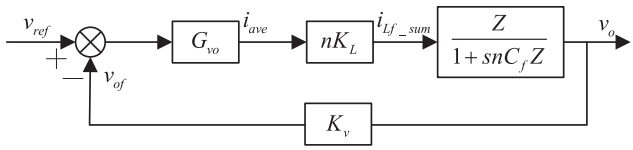


Fig. 8. Control block diagram of OV loop.

In order to ensure the stability of ISOP inverter system, the equivalent input impedance of each inverter module should present positive resistance characteristics, i.e.,

$$Z_{\mathrm{in}} = \frac{R_n \cdot R_{\mathrm{IVS}j}}{R_n - R_{\mathrm{IVS}j}} > 0, \quad (j = 1, 2, \ldots, n). \tag{28}$$

Hence, the condition for stability is

$$R_n > R_{\mathrm{IVS}j}, \quad (j = 1, 2, \ldots, n). \tag{29}$$

Substitution of (19) and (26) into (29), yields

$$G_{vd} > G_{vd\min} = \frac{n}{K_f \cdot V_{\mathrm{in}}}. \tag{30}$$

It can be seen that the gain of IVS loop compensator must satisfy (30) so that the ISOP inverter system with IVS control strategy is stable.

2) Design of output voltage regulator (OVR): As to the design of the OV loop, we can get following equation from Fig. 6(b):

$$\begin{aligned} i_{\mathrm{reg}} = {} & \frac{1}{n} \cdot \sum_{j=1}^{n} i_{\mathrm{reg}j} = \frac{1}{n} \cdot \sum_{j=1}^{n} (i_{\mathrm{ave}} \cdot v_{\mathrm{dev}j}) \\ = {} & \frac{1}{n} \cdot i_{\mathrm{ave}} \cdot G_{vd} \cdot (n \cdot V_{\mathrm{in\_ref}} - K_f \cdot \sum_{j=1}^{n} v_{cdj}) \\ = {} & \frac{1}{n} \cdot i_{\mathrm{ave}} \cdot G_{vd} \cdot (n \cdot V_{\mathrm{in\_ref}} - K_f \cdot V_{\mathrm{in}}) = 0. \end{aligned} \tag{31}$$

Then combining formula (31) and Fig. 6(b), we can derive the equivalent control block of OV loop transfer function for each inverter as shown in Fig. 8.

Thus, the loop gain at full resistive load takes the following form:

$$T(s) = \frac{n \cdot G_{vo}(s) \cdot K_v \cdot K_L \cdot R_L}{1 + s \cdot n \cdot R_L \cdot C_f}. \tag{32}$$

While

$$R_L = \frac{V_o^2}{P_{\mathrm{total}}} = \frac{V_o^2}{n \cdot p_{o-\mathrm{mod}}}. \tag{33}$$

Here, P_{total} and P_{o_mod} represent overall system output power and single module output power under full resistive load, respectively. Since the power of the standard module is defined, we can derive $n \cdot R_L$ with constant value as

$$R_{\mathrm{mod}} = n \cdot R_L = \frac{V_o^2}{p_{o-\mathrm{mod}}}. \tag{34}$$

So (32) could be simplified as

$$T(s) = \frac{G_{vo}(s) \cdot K_v \cdot K_L \cdot R_{\mathrm{mod}}}{1 + s \cdot C_f \cdot R_{\mathrm{mod}}}. \tag{35}$$

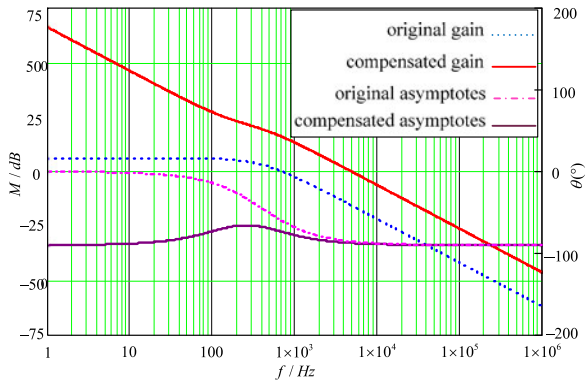


Fig. 9. OV loop gains with and without compensation.

Here, $K_L = 5, K_v = 0.031, V_o = 115\,\text{V}$, and $P_{o\_\text{mod}} = 1\,\text{kW}$. Substituting these parameters into (35) and suppose $G_{vo}(s)$ is equal to 1, we can acquire the OV loop gains without compensation as shown in Fig. 9, from which we can find that the uncompensated cutoff frequency is low as about 700 Hz. For the sake of improving the tracking precision of the OV, we apply a PI regulator. The hysteresis current control inverter has a broad distribution of harmonics in the OV and its switching frequency is variable. Denoting its sampling frequency by f_k, the hysteresis current control inverter can be equivalent to the pulse width modulation (PWM) inverter whose switching frequency is a quarter of f_k [37], [38]. Suppose the sampling frequency of the inverter is 100 kHz. Then, the switching frequency of the PWM inverter, which is equivalent from the hysteresis current control inverter, is 25 kHz. One-fifth of this frequency, i.e., $f_c = 5$ kHz, is set as the cutoff frequency of the compensated OV loop. From Fig. 9, we can find the magnitude of the uncompensated loop gain as -15.6 dB at 5 kHz. Thus, the compensator should have a gain of 15.6 dB at 5 kHz. The inverted zero of the compensator is chosen at 500 Hz, one-tenth of the cutoff frequency. Then, the transfer function of the PI regulator can be derived as

$$G_{vo}(s) = 6 + \frac{6250}{s}. \tag{36}$$

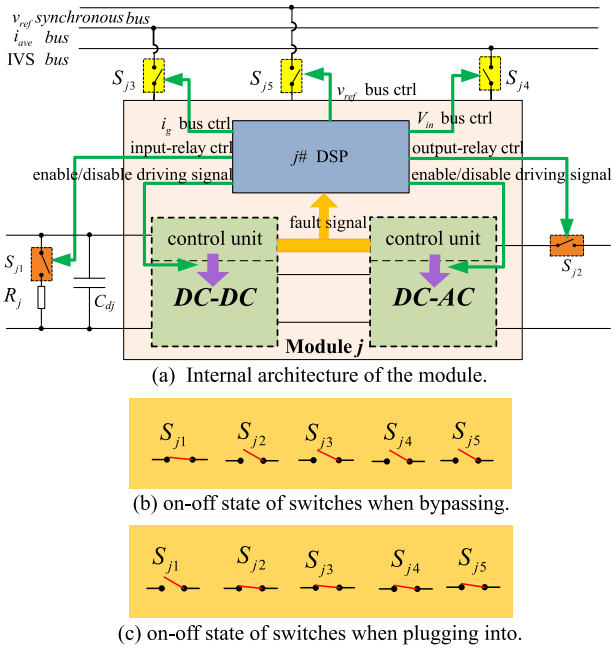
With adoption of the PI regulator, the compensated loop gain has a cutoff frequency of 5 KHz with a phase margin of 95°, which means the superior performance of the control system.

IV. Redundant Control to Improve the Reliability of the System

A. Proposed Hot-Plugging Solution for ISOP Inverter System

With the control loops dispersed into each module and the buses communication, distributed control of the system is obtained. Then, the hot swap could be on the way. That is the second step for the achievement of the redundancy.

Owning to series connection at the input terminal, the hot-plugging technique for ISOP inverter system is quite different from that of mature IPOP inverter system in which the failure modules are removed directly from the system when malfunctions happen. Here for ISOP architecture we introduce the input



(a) Internal architecture of the module.

(b) on-off state of switches when bypassing.

(c) on-off state of switches when plugging into.

Fig. 10. Internal architecture of the module and ON–OFF state of switches during the course of hot swap. (a) Internal architecture of the module. (b) ON–OFF state of switches when bypassing. (c) ON–OFF state of switches when plugging into.

relays $S_{11} - S_{n1}$ and output relays $S_{12} - S_{n2}$ in Fig. 1 to bypass the faulty modules other than to cut them off. Further, we should also introduce the signal switches S_{j3}, S_{j4} and S_{j5} (referring to Fig. 3) together with relays S_{j1} and S_{j2} to carry out the bypassing or plugging into of the module.

Fig. 10(a) shows the internal architecture of the module. The switches S_{j1} and S_{j2} are realized by the power relay which has its inherent delay time, and the signal switches S_{j3}, S_{j4}, S_{j5} are realized by the analog switch CD4051 which can respond almost at once since its action delay is only several hundred nanosecond. To realize the hot plugging, we need to regulate S_{j1} ON, S_{j2}, S_{j3}, S_{j4} and S_{j5} OFF to bypass the broken-down module [referring to Fig. 10(b)], while control S_{j1} OFF, S_{j2}, S_{j3}, S_{j4} and S_{j5} ON to plug into the new one [referring to Fig. 10(c)]. The DSP TMS320F28027 monitors the operation of the module, and will trigger the hot-plugging process when a fault signal is detected. Besides the ON–OFF signal of the switches, the DSP has to transfer the enable/disable driving signal to control unit of the two stages of each module. The operating time sequence of these signals is intricate and is very crucial to the smooth transmission of hot-plugging process. The detailed timing sequence will be shown in the next section.

B. Timing Sequence of System Operation

In this section, timing sequence will be introduced. The whole logic is controlled by a DSP chip. And the procedure involves two parts as bypassing and plugging into.

When a fault signal is detected, DSP will trigger the bypassing procedure. The first thing we should execute immediately is to lock the driving signals of both the dc–dc and dc–ac stage of

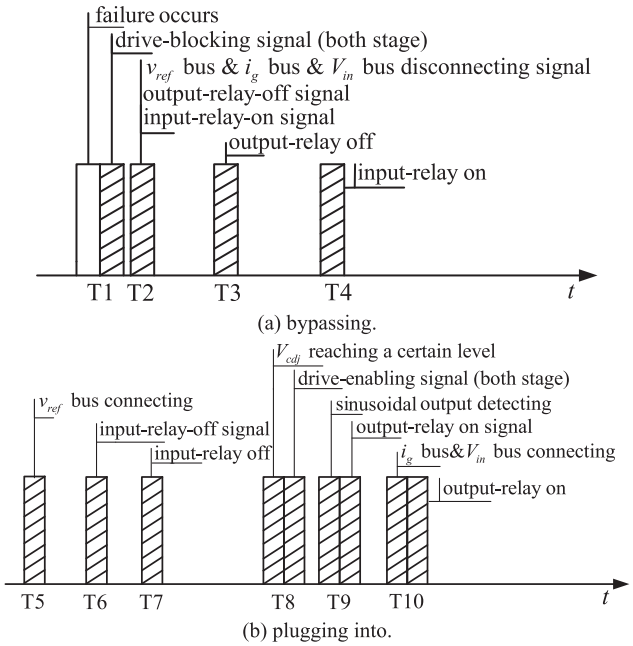
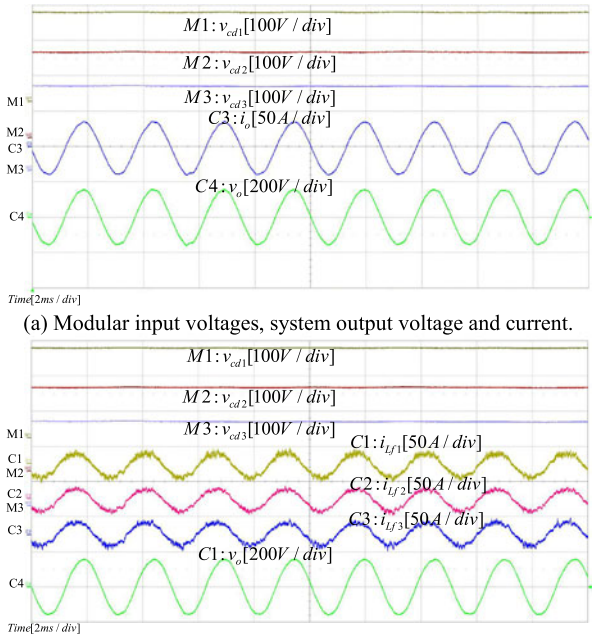


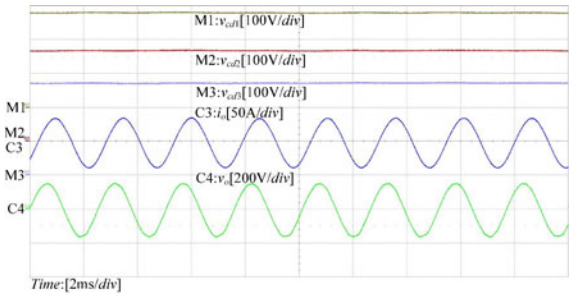
Fig. 11. Timing sequence illustration of hot plugging. (a) Bypassing. (b) Plugging into.



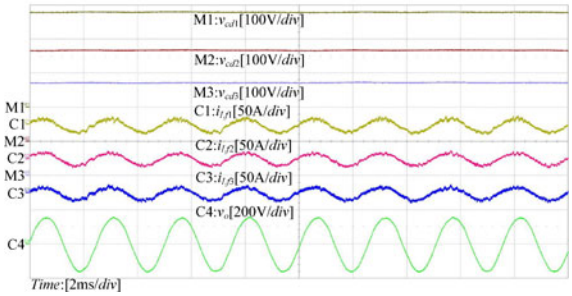
(a) Modular input voltages, system output voltage and current.

(b) Modular input voltages, output inductor currents and system output voltage.

Fig. 12. Steady-state waveforms at full resistive load. (a) Modular input voltages, system OV and current. (b) Modular input voltages, output inductor currents and system OV.



(a) Modular input voltages, system output voltage and current.



(b) Modular input voltages, output inductor currents and system output voltage.

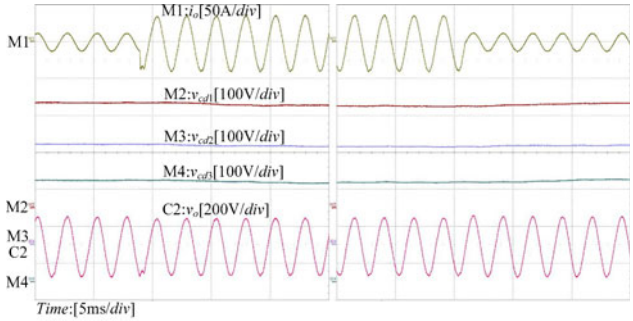
Fig. 13. Steady-state waveforms at full inductive load. (a) Modular input voltages, system OV and current. (b) Modular input voltages, output inductor currents and system OV.

the failure module at T1 [see Fig. 11(a)] in case of its adverse impact on the system. Then, almost simultaneously at T2 we need to give the disconnecting signal of switches as S_{j3}, S_{j4} and S_{j5}, which will release connection of control units from the $i_g\ bus$, IVS bus, and $v_{\rm ref}bus$. And the output-relay (S_{j2})-OFF and input-relay(S_{j1})-ON signal are also provided at the same time. The switches S_{j3}, S_{j4} and S_{j5} turn OFF almost at once, while, due to the delay of the relay operation, the output and input relay actually react at T3 and T4, respectively. After a while from T4, the system returns to the steady state and the bypassing course ends.

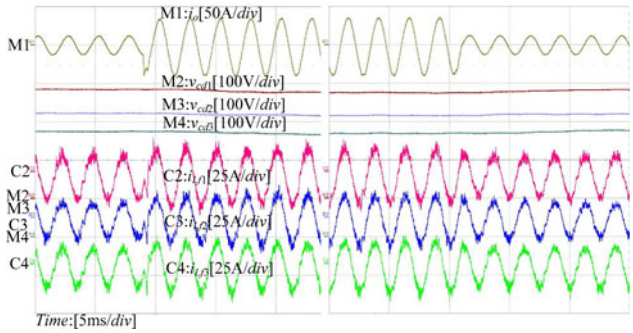
As long as a healthy module is ready, DSP could give the order to put it into the system. First, the DSP sends the signal to turn ON S_{j5} to connect its control unit with the $v_{\rm ref}bus$ at T5 to make sure the new module realize bus signal synchronization. After turning OFF the input relay at T7 [see Fig. 11(b)], the voltage of the input dividing capacitor begins to rise. In order to accelerate the plugging-into process to a certain extent, the drive-enabling signals of both stages of the new module should be given when the input voltage reaches a certain level. Once the drive-enabling signals are offered, the plugging-into module begins to generate OV. When DSP regards the OV to be sinusoidal at T9, the output-relay-on signal will be provided. As the output-relay is just about to react at T10, the bus ($i_g\ bus$ and $V_{\rm in}\ bus$) connection signals are given. Hence, the hot-plugging terminates and the system goes back to normal.

V. Experimental Results

To verify the effectiveness and validity of the proposed control scheme, a 3-kVA prototype of three-module ISOP inverter system is fabricated and tested in the lab. The specifications are as follows: system input voltage: $V_{\rm in} = 810(\pm 10\%)$VDC, modular input voltage: $V_{cd} = 270(\pm 10\%)$VDC, OV: $V_o =$ 115 VAC/400 Hz, modular dc link voltage: $V_{\rm dc} = 180$ VDC, modular output power: 1 kVA, Switching frequency of the

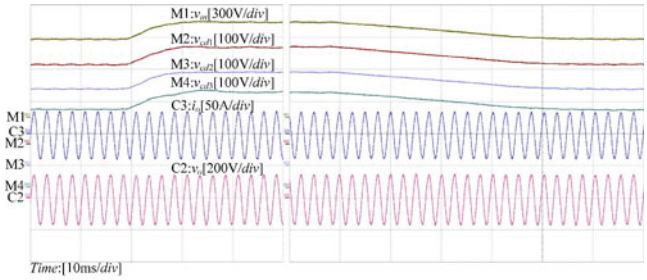


(a) System output current, modular input voltages and system output voltage.

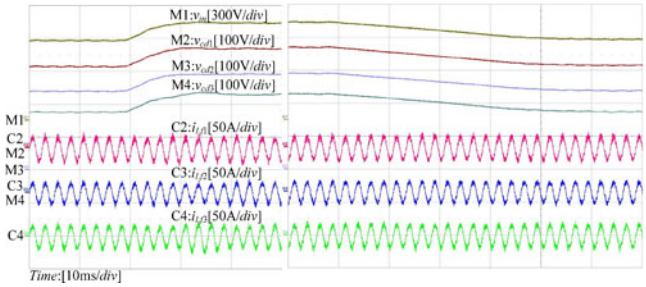


(b) System output current, modular input voltages and output inductor currents.

Fig. 14. Experimental waveforms under step-load condition. (a) System output current, modular input voltages and system OV. (b) System output current, modular input voltages and output inductor currents.



(a) System input voltage, modular input voltages, system output voltage and current.



(b) System input voltage, modular input voltages and output inductor currents.

Fig. 15. Experimental waveforms under step-line condition. (a) System input voltage, modular input voltages, system OV and current. (b) System input voltage, modular input voltages and output inductor currents.

dc-dc stage: 100 kHz, Switching frequency of the dc–ac stage: 25 kHz.

The devices of the module and their values are as follows:

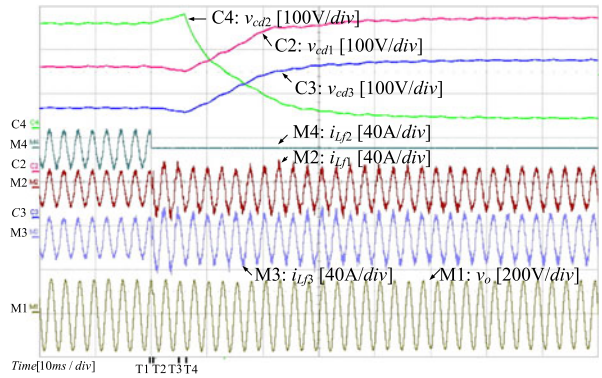
Devices of the dc–dc stage: input dividing capacitor: $C_d = 1000\ \mu$F, switching device: IRFP460, rectifier diode: DSEI30–06, output filter inductor: $L_{\rm dc} = 0.26$ mH, output filter capacitor: $C_{\rm dc} = 1640\ \mu$F(820μF $\times$ 2).

Devices of the dc–ac stage: switching device: IXTQ42N25P, output filter inductor: $L_f = 0.7$ mH, output filter capacitor: $C_f = 30\ \mu$F.

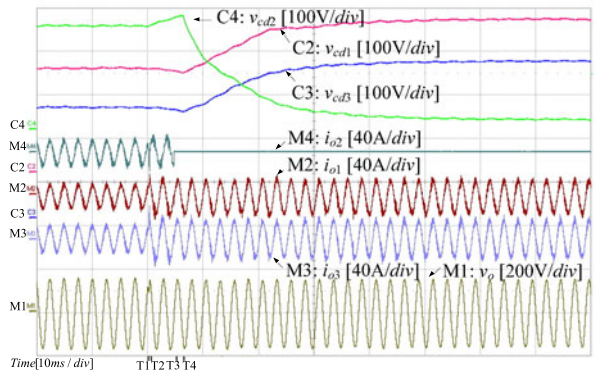
Figs. 12 to 15 give the experimental waveforms of the aforementioned distributed control strategy. From Figs. 12 and 13 which show the waveforms at full resistive and inductive load, we can see that IVS and OCS are achieved and the distributed method is effective at steady state.

Fig. 14 detects the transient response of the system at the nominal input voltage when the load current steps up and down between one-third load and full load. Also, Fig. 15 presents the transient process of the system at full resistive load when the input voltage steps up and down between 729 V (90% rated input voltage) and 891 V (110% rated input voltage). From the two figures, we can find that regardless of perturbation at the input voltage or the load, IVS and OVS can be achieved effectively and the distributed scheme is valid at dynamic state.

After distributed control realized, fault tolerance could be implemented to promote the reliability of the system. Following graphs present the experimental results of the proposed redundant method. Here module 2 is regarded as the hot-swap module.

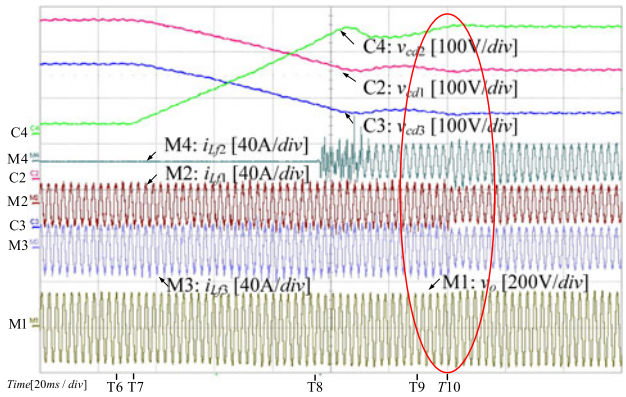


(a) Modular input voltages, output inductor currents and system output voltage.

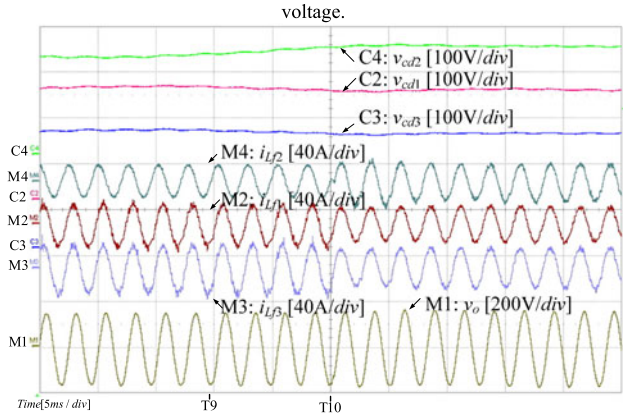


(b) Modular input voltages, output currents and system output voltage.

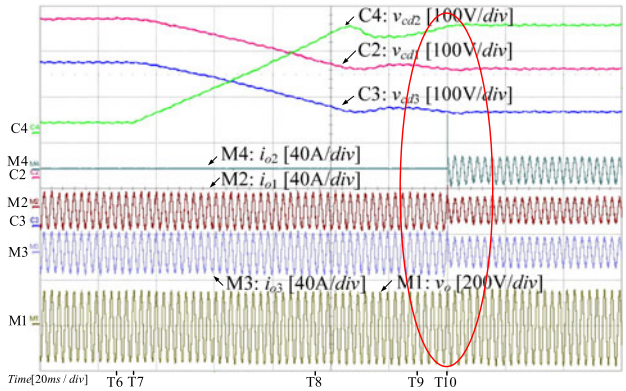
Fig. 16. Bypassing. (a) Modular input voltages, output inductor currents and system OV. (b) Modular input voltages, output currents and system OV.



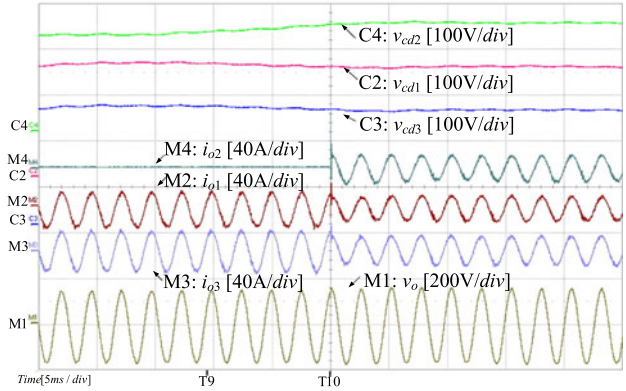
(a) Modular input voltages, output inductor currents and system output voltage.



(b) Zoomed area of T10 in (a).



(c) Modular input voltages, output currents and system output voltage.



(d) Zoomed area of T10 in (c).

Fig. 17. Plugging into the system. (a) Modular input voltages, output inductor currents and system OV. (b) Zoomed area of T10 in (a). (c) Modular input voltages, output currents and system OV. (d) Zoomed area of T10 in (c).

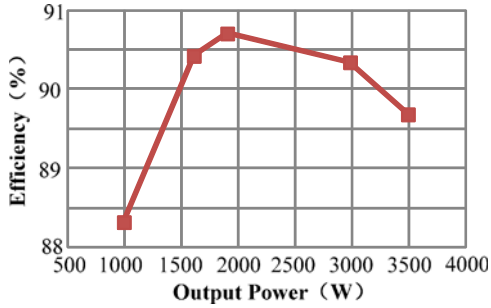


Fig. 18. Efficiency curve of the overall converter.

Fig. 16 shows the waveforms of the bypassing process. After blocking the driving signals of dc–dc and dc–ac stage, the inductor current i_{L2} reduces sharply to zero at T1. Due to the delay of the input-relay action, the voltage of the dividing capacitor V_{dc2} increases slightly, while the other two capacitors decrease briefly. When the output-relay finally reacts at T3, the output current i_{o2} drops to zero immediately. As the input-relay reacts at T4, the dividing capacitor C_{d2} discharges through the resistor and its voltage falls down, while the other two capacitors charge and their voltages goes up. In a minute, the system returns to steady state and the bypassing process ends. It can be seen that the smooth transition is achieved during the cause of the transient.

Fig. 17 shows the waveforms of the plugging-into procedure. Fig. 17(a) shows the modular input voltages, output inductor currents, and system OV. A new healthy module, module 2, is actually put into the system at T10, and Fig. 17(b) shows the zoomed area of red circle in (a). We can see that the system comes back to the normal state in time. Fig. 17(c) shows the modular input voltages, output currents, and system OV. Also the Fig. 17(d) is the zoomed area of T10 in (c). We can see that the module burdens the system load promptly, and we can barely see any voltage fluctuate from the OV. So the smooth transition is also realized here and the hot-plugging is finished.

It is noted that if one module fails, the other modules should be able to handle the increased voltage. Does the choice and design of the switching device at the input terminal have any influence on the overall converter efficiency? Let's talk about the issue. First, for the three-module system in the experiment of this paper, the input voltage of each module changes from 270 to 405 V when one module fails and retreats from the system. While MOSFET optional voltage level is generally as follows: below 100, 250, 500, 650, and 650 V above. So we need to choose 500-V MOSFET no matter whether the three module or the two module running. Here, we choose IRFP460 whose voltage level is 500 V. Second, for the general N + 1 redundant system (where N is a slightly larger number), the input voltage of each module changes little when one failure module is bypassed from the system. It is thus obvious that the choice and design of the switching device has little impact on converter efficiency. Fig. 18 give the efficiency curve of the overall converter and the system efficiency at rated power is about 90.3%.

VI. Conclusion

Two vital tasks have to be concerned for ISOP inverter system. One is to achieve power balance, i.e., to ensure IVS and OCS for the whole system. The other is to realize the redundancy so as to enhance the reliability of the system authentically. For the sake of fulfilling the both crucial missions, this paper first puts forward the compound control to obtain IVS and OCS for the system. Based on the control conception, the article then comes up with a novel distributed control method, in which all the control elements have been dispersed into every module to get the fully modular system. As to the distributed control implementation, the decoupling relationship of the control loops is analyzed and the loop design is also given. On the basis of the distributed configuration, the power relays and signal switches are inserted into the main circuit and control units, respectively, to execute the hot swap. It is worth noting that the bypassing way is proposed to realize the exit of the faulty module, and the detailed timing sequence of system operation is presented as well to accomplish the redundancy for the ISOP inverter system.

References

[1] R. Ayyanar, R. Giri, and N. Mohan, "Active input-voltage and load-current sharing in input-series and output-parallel connected modular dc-dc converters using dynamic input-voltage reference scheme," *IEEE Trans. Power Electron.*, vol. 19, no. 6, pp. 1462–1473, Nov. 2004.

[2] Y. Huang, C. K. Tse, and X. Ruan, "General control considerations for input-series connected DC/DC converters," *IEEE Trans. Circuits Syst.*, vol. 56, no. 6, pp. 1286–1296, Jun. 2009.

[3] T. Qian and B. Lehman, "Buck/half-bridge input-series two-stage converter," *IET Power Electron.*, vol. 3, no. 6, pp. 965–976, Nov. 2010.

[4] A. J. B. Bottion and I. Barbi, "Input-series and output-series connected modular output capacitor full-bridge PWM DC-DC converter," *IEEE Trans. Power Electron.*, vol. 62, no. 10, pp. 6213–6221, Oct. 2015.

[5] D. Sha, Z. Guo, T. Luo, and X. Liao, "A general control strategy for input-series–output-series modular DC–DC converters," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3766–3775, Jul. 2014.

[6] X. Hu and C. Gong, "A high gain input-parallel output-series DC-DC converter with dual coupled inductors," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1306–1317, Mar. 2015.

[7] Z. Guo, D. Sha, X. Liao, and J. Luo, "Input-series-output-parallel phase-shift full-bridge derived DC–DC converters with auxiliary LC networks to achieve wide zero-voltage switching range," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5081–5086, Oct. 2014.

[8] S. Sheng, P. Li, and B. Lehman, "Parallel operation of digital controlled modified sine wave inverters," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2013, pp. 3440–3447.

[9] S. B. Bekiarov and A. Emadi, "Uninterruptible power supllies: Classification, operation, dynamics and control," in *Proc. IEEE Annu. Appl. Power Electron. Conf. Expo.*, 2002, pp. 597–604.

[10] M. Borrega, L. Marroyo, R. Gonźalez, J. Balda, and J. L. Agorreta, "Modeling and control of a master–slave PV inverter with N-paralleled inverters and three-phase three-limb inductors," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2842–2855, Jun. 2013.

[11] G. P. Ladrón, V. Cárdenas, and G. Espinosa, "Analysis and implementation of a mater-slave control based on a passivity approach for parallel inverters operation," in *Proc. IEEE Int. Power Electron. Congr.*, Pucbla, Mexico, 2006, pp. 1–5.

[12] Y. Zhang, M. Yu, F. Liu, and Y. Kang, "Instantaneous current-sharing control strategy for parallel operation of UPS modules using virtual impedance," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 432–440, Jan. 2013.

[13] X. Sun, Y. S. Lee, and D. Xu, "Modeling, analysis and implementation of parallel multi-inverter system with instantaneous average –current-sharing scheme," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 844–856, May 2003.

[14] Y. Xing, L. Huang, and Y. Yan, "Redundant parallel control for current regulated inverters with instantaneous current sharing," in *Proc. IEEE Annu. Power Electron. Spec. Conf.*, 2003, pp. 1438–3658.

[15] T. Fang, X. Ruan, L. Xiao, and A. Liu, "An improved distributed control strategy for parallel inverters," in *Proc. IEEE Annu. Power Electron. Spec. Conf.*, 2008, pp. 3500–3505.

[16] T. F. Wu, Y. E. Wu, H. M. Hsieh, and Y. K. Chen, "Current weighting distribution control strategy for multi-inverter systems to achieve current sharing," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 160–168, Jan. 2007.

[17] J. M. Guerrero, J. Matas, L. Vicuña, M. Castilla, and J. Miret, "Wireless-control strategy for parallel operation of distributed-gernation inverters," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1461–1470, Oct. 2014.

[18] K. Brabandere, B. Bolsens, J. Keybus, A. Woyte, J. Driesen, and R. Belmans, "A voltage and frequency droop control method for parallel inverters," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1107–1115, Jul. 2007.

[19] J. Matas, M. Castilla, L. Vicuña, J. Miret, and J. Vasquez, "Virtual impedance loop for droop-controlled single-phase parallel inverters using a second-order general-integrator scheme," *IEEE Trans. Power Electron.*, vol. 25, no. 12, pp. 2993–3002, Dec. 2010.

[20] M. Hua, H. Hu, Y. Xing, and J. M. Guerrero, "Multilayer control for inverters in parallel operation without intercommunications," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3651–3663, Aug. 2012.

[21] J. C. Vasquez, J. M. Guerrero, M. Savaghebi, J. E. Garcia, and R. Teodorescu, "Modeling, analysis, and design of stationary-reference-frame droop-controlled parallel three-phase voltage source inverters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 4, pp. 1271–1280, Apr. 2013.

[22] B. H. Jeong, J. C. Park, G. H. Choe, and J. S. Cho, "Parallel operation control of N + 1 redundant inverter system," in *Proc. IEEE Annu. Power Electron. Spec. Conf.*, 2006, pp. 1–6.

[23] T. F. Wu, H. M. Hsieh, Y. E. Wu, and Y. K. Chen, "Parallel-inverter system with failure isolation and hot-swap features," *IEEE Trans. Ind. Electron.*, vol. 43, no. 5, pp. 1329–1340, Sep./Oct. 2007.

[24] T. B. Lazzarin, G. A. T. Bauer, and I. Barbi, "A control strategy for parallel operation of single-phase voltage source inverters: Analysis, design and experimental results," *IEEE Trans. Ind. Electron.*, vol. 60, no. 6, pp. 2194–2204, Jun. 2013.

[25] B. M. Song, R. McDowell, A. Bushnell, and J. Ennis, "A three-level DC–DC converter with wide-input voltage operations for ship-electric-power-distribution systems," *IEEE Trans. Plasma Sci.*, vol. 32, no. 5, pp. 1856–1863, Oct. 2004.

[26] A. D. Cheok, S. Kawamoto, T. Matsumoto, and H. Obi, "High power AC/DC converter and DC/AC inverter for high speed train applications," in *Proc. IEEE TENCON*, 2000, pp. 423–428.

[27] J. W. Kim, J. S. You, and B. H. Cho, "Modeling, control, and design of input-series–output-parallel-connected converter for high-speed-train power system," *IEEE Trans. Ind. Electron.*, vol. 48, no. 3, pp. 536–544, Jun. 2001.

[28] T. Fang, X. Ruan, and C. K. Tse, "Control strategy to achieve input and output voltage sharing for input-series-output- series connected inverter system," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1585–1596, Jun. 2010.

[29] D. Sha, G. Xu, and X. Liao, "Control strategy for input-series-output-series high-frequency AC-link inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 5283–5292, Nov. 2013.

[30] M. F. Kangarlu and E. Babaei, "A generalized cascaded multilevel inverter using series connection of submultilevel inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 625–636, Feb. 2013.

[31] R. Selvamuthukumaran, A. Garg, and R. Gupta, "Hybrid multicarrier modulation to reduce leakage current in a transformerless cascaded multilevel inverter for photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 1779–1783, Apr. 2015.

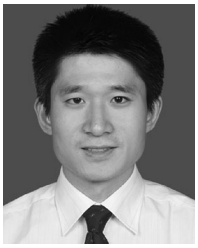
[32] S. Maríethoz, "Systematic design of high-performance hybrid cascaded multilevel inverters with active voltage balance and minimum switching losses," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3100–3113, Jul. 2013.

[33] K. Zhuang and X. Ruan, "Control strategy to achieve input voltage sharing and output current sharing for input- series-output-parallel inverter," in *Proc. IEEE Annu. Power Electron. Spec. Conf.*, 2008, pp. 3655–3658.

[34] W. Chen, K. Zhuang, and X. Ruan, "A input-series-and output-parallel-connected inverter system for high-input-voltage applications," *IEEE Trans. Power Electron.*, vol. 24, no. 9, pp. 2127–2137, Sep. 2009.

[35] W. Chen and X. Ruan, "An improved control strategy for input-series and output-parallel inverter system at extreme conditions," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2010, pp. 2096–2100.

[36] D. Sha, Z. Guo, and X. Liao, "Control strategy for input-series–output-parallel high-frequency AC link inverters," *IEEE Trans. Ind. Electron.*, vol. 59, no. 11, pp. 4101–4111, Nov. 2012.
[37] G. Venkataramanan, D. M. Divan, and T. M. Jahns, "Discrete pulse modulation strategies for high-frequency inverter systems," *IEEE Trans. Power Electron.*, vol. 8, no. 3, pp. 279–287, Jul. 1993.
[38] G. Venkataramanan and D. M. Divan, "Pulse width modulation with resonant dc link converters," *IEEE Trans. Ind. Appl.*, vol. 29, no. 1, pp. 113–120, Jan./Feb. 1993.



Tianzhi Fang (M'13) was born in Jiangsu Province, China, in 1977. He received the B.S. and Ph.D. degrees in electrical engineering from the Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 1991 and 1996, respectively. He received the B.S. degree in electrical engineering and automation and the Ph.D. degree in electrical engineering from the NUAA, Nanjing, China, in 2000 and 2009, respectively, and the M.S. degree in control theory and engineering from Jiangsu University, Zhenjiang, China, in 2003.

In 2009, he joined the Faculty of the College of Automation Engineering, NUAA, where he is currently an Associate Professor. His main research interests include series–parallel inverters, grid-connected inverter, and power electronics system integration.

Le Shen was born in Jiangsu Province, China, in 1989. He received the B.S. degree in electrical engineering and automation from the Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2013, where he is currently working toward the M.S. degree in electrical engineering.

His main research interests include inverters and power electronics system integration.

Wei He was born in Jiangsu Province, China, in 1992. She received the B.S. degree in electrical engineering and automation from the Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 2014, where she is currently working toward the M.S. degree in electrical engineering.

Her main research interests include inverters and power electronics system integration.

Xinbo Ruan (M'97–SM'02–F16) was born in Hubei Province, China, in 1970. He received the B.S. and Ph.D. degrees in electrical engineering from the Nanjing University of Aeronautics and Astronautics (NUAA), Nanjing, China, in 1991 and 1996, respectively.

In 1996, he joined the Faculty of Electrical Engineering, Teaching and Research Division, NUAA, where he became a Professor in the College of Automation Engineering in 2002 and has been engaged in teaching and research in the field of power electronics. From August to October 2007, he was a Research Fellow in the Department of Electronic and Information Engineering, Hong Kong Polytechnic University, Hong Kong, China. Since March 2008, he has been also with the College of Electrical and Electronic Engineering, Huazhong University of Science and Technology, China. He is a Guest Professor with Beijing Jiaotong University, Beijing, China, Hefei University of Technology, Hefei, China, and Wuhan University, Wuhan, China. He is the author or coauthor of seven books and more than 200 technical papers published in journals and conferences. His main research interests include soft-switching dc–dc converters, soft-switching inverters, power factor correction converters, modeling the converters, power electronics system integration, and renewable energy generation system.

Dr. Ruan received the Delta Scholarship by the Delta Environment and Education Fund in 2003 and was appointed as the Special Appointed Professor of the Chang Jiang Scholars Program by the Ministry of Education, China, in 2007. From 2005 to 2013, he had been serving as the Vice President of the China Power Supply Society, and since 2014, he has been serving as the Vice Chair of the Technical Committee on Renewable Energy Systems within the IEEE Industrial Electronics Society. He is currently an Associate Editor for the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE TRANSACTIONS ON POWER ELECTRONICS, IEEE JOURNAL OF EMERGING AND SELECTED TOPICS ON POWER ELECTRONICS, and IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS-II.