Efficiency/Cost Trade-off Design of a Multiple-Active-Bridge Converter for Smart Transformer

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***Abstract*—The modular Smart Transformer (ST) is composed by several basic converters rated for lower voltage and power. In this paper the quadruple active bridge (QAB) is used as the basic block for the modular ST. In this application, the efficiency and cost are the most important design parameters. Therefore, the paper focus on the design of the converter, with the aim to optimize its efficiency, taking the cost into consideration. To do so, the losses of all components are carefully modeled and a computer-aided design is used, where an algorithm to calculate the losses and cost is developed, allowing to perform multi-objective optimization. Additionally, Silicon IGBTs and Silicon Carbide MOSFETs are considered for the design and the performance of the converter using both semiconductors technology is compared. Experimental results obtained for the optimized 20 kW QAB converter has shown an efficiency of 97.5%.**

I. Introduction

Over the past years, many researches have been focused on efficiency improvement of dc-dc converters and several design optimization methods and power converter topologies have been discussed [1]–[9]. Among the most investigated topologies, the Dual Active Bridge (DAB) converter [10], composed of two active bridges connected through a high frequency transformer, is highlighted as a high performance solution, because of its soft-switching feature and high power density. Therefore, this converter has been widely used in application with different power and voltage levels, mainly those that required high efficiency.

In Smart Transformer (ST) application, the DAB converter became a standard solution for the dc-dc stage, mainly because of its simple power flow control [1]. However, not only the efficiency, but also the cost plays a very important role during the design and the topologies choice for the system implementation. Recent investigations have shown the economic advantages of the Multiple Active Bridge (MAB) over the DAB, when applied to ST [11], [12]. The MAB is an extension of the DAB converter, where more bridges are coupled to the same multiwinding high frequency transformer (HFT). Consequently, employing the MAB instead the DAB in ST, the total number of HFT, LV cells, as well as auxiliary components (communication system and auxiliary power supply) are reduced, resulting in lower cost. In addition to that, the MAB operates similarly to the DAB, preserving the same advantages and then high performance is also expected.

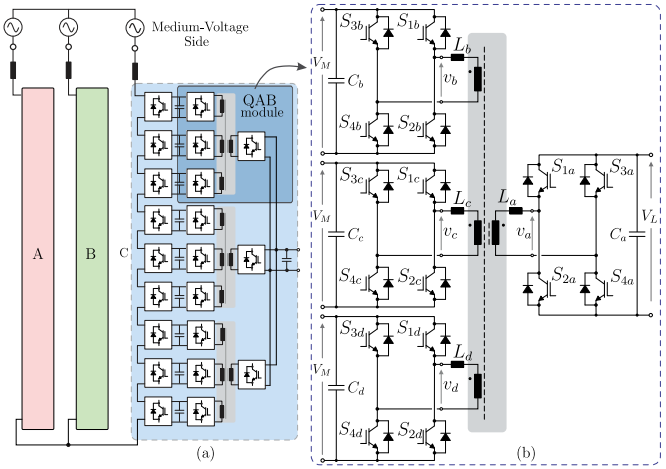

Figure 1. (a) Modular ST architecture using the QAB converter as a basic module of the dcdc stage. (b) QAB converter topology.

On the other hand, most of the publications related to this converter were focused on the power control between the bridges, and little attention was paid to the design and efficiency improvement. In [13], the design of a MAB converter based on three active bridges (TAB) is presented, but a peak efficiency of only 91.5% was obtained for the built converter. Similarly, a MAB converter is designed and implemented in [14], [15], where a maximum efficiency of 92% is reported. The high performance of the MAB converter has not yet been demonstrated in literature.

In this context, this paper presents the design of a MAB converters, with the aim to optimize the efficiency, but considering the cost of the converter. To do so, a computer-aided design is used, where the parameters are properly selected and the losses on the main power components are carefully calculated. Additionally, Silicon IGBTs (Si-IGBT) and Silicon Carbide MOSFETs (SiC-MOSFETS) are considered in the design, in order to reduce the switching and conduction losses and verify the performance of the converter using different semiconductors technology. Furthermore, the cost of the components are considered, allowing to perform a multi-objective (efficiency

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Table I
SPECIFICATION OF THE GRID AND QAB CONVERTER

Rated Power	MVAC	LVAC	Grid frequency
500 kVA	10 kV	400 V	50 Hz
QAB Converter Specification			
Rated Power	Input Voltage	Output Voltage	Switching freq.
20 kW	800 V	700 V	20 kHz

and cost) optimization

The economical advantages of the MAB in ST application was proved in [12], and the main goal of this paper is to validate theoretically and experimentally its high performance in terms of efficiency, demonstrating the feasibility of the MAB in this application.

The paper is divided as follows: in section II, the ST concept is briefly introduced, where its characteristics and requirements used for the MAB designed is presented. Then, the MAB converter is introduced in Section III, where its main equations used on the design are provided. In section IV, the design methodology is presented, where the components are selected, the losses are calculated and theoretical efficiency is estimated.

II. MODULAR SMART TRANSFORMER ARCHITECTURE

Smart Transformer (ST) is a power electronics-based system usually composed of three conversion stages (AC-DC, DC-DC and DC-AC) with advanced control and communication functionality [1], [2]. Because of its high control performance, it became a promising system to solve the current problems of the modern distribution system, and its advantages and benefits in distribution system have been discussed in [1], [2]. Different architectures can be used to implement the ST [1], but the modular one has shown more advantages, because it enables the fault tolerance. Using this approach, the dc-dc stage is composed by several basic dc-dc converters rated for low power and low voltage. In this work, the MAB converter is employed as a basic cell, where four bridges (named quadruple active bridge - QAB) are used, as shown in Fig. 1. The asymmetric configuration, where three bridges are connected to the MV side and one to the LV side (see. Fig. 1), is more advantageous than the symmetric connection (two bridges in each side), because the total number of HFT and LV cells are reduced, while the semiconductors with lower blocking voltage can be used in the MV cells [12]. Therefore, this configuration is chosen to be used in this work.

A typical ST specification for distribution system is presented in Table I, as well as the specification of the QAB converter, and the QAB converter design is carried out based on these specifications.

III. OPERATION PRINCIPLE OF THE MAB CONVERTER

The QAB is composed of four active bridges and for the analysis, each of them is denoted by the letters a, b, c and d. The elements of the bridges have sub-index $i = \{a,b,c,d\}$ to indicate the bridge the element belongs to. To analyze the converter, an equivalent circuit based on the Y-model and depicted in Fig. 2 (a) is used, in which the bridges are replaced

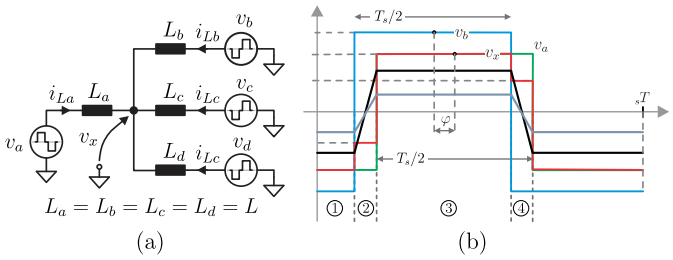

Figure 2. Model of the QAB converter and main waveforms, using the PSM.

by rectangular voltage sources (v_a, v_b, v_c and v_d). The voltage at the central point v_x and the current slope of each inductor are given by (1) and (2), respectively, where $k = \{a,b,c,d\}$.

To modulate the converter, the Phase-Shift Modulation (PSM) strategy is employed. Using this modulation scheme, rectangular voltages v_a, v_b, v_c and v_d with phase shift φ_a, φ_b, φ_c and φ_d, respectively, and constant switching frequency f_s are applied to the transformer. The power is controlled by the phase difference among the bridges and it can be generally described in (3), where, $i = a,b,c,d$ and $k = a,b,c,d$, according to [16], [17]. The main waveform of the PSM is shown in Fig. 2 (b).

$$v_x = \frac{v_a + v_b + v_c + v_d}{4} \tag{1}$$

$$\frac{di_{Lk}}{dt} = \frac{(v_k - v_x)}{L} \tag{2}$$

$$P_{ik} = \frac{V_M V_L}{2\pi f_s L n}\varphi_{ik}\left(1 - \frac{|\varphi_{ik}|}{\pi}\right), \varphi_{ik} = \varphi_i - \varphi_k \tag{3}$$

The PSM is characterized by ZVS turn-on, but this features depends on the input and output voltages relation and also on the load. In this application, the input voltage of the QAB (all the three cells) is regulated by the first stage of the ST, i.e. the MV rectifier, while the QAB controls the output voltage. As the input and output voltage are considered constant, the converter can be properly designed to work with ZVS operation for its entire range of operation. Consequently, this scheme offers several advantages for the converter operation.

In ST application, equal power sharing is normally assumed (i.e. power balanced condition), and the MV cells operate with the same phase shift angle. In this condition, there is no circulating power among the MV cells, but only power exchange between the MV and LV sides. Consequently, the equation (3) can simplified to (4), where φ is the phase-shift angle between the MV cells and LV cell and L_{eq} is the equivalent inductance seen by the LV cell. Thus, from this equation, the total required inductance is calculated. As can be noticed in (3) and (4), the input and output voltages are constant, as well as the switching frequency (f_s); hence, the power transference depends only the equivalent inductance and the nominal phase-shift angle. The choice of the nominal phase-shift is critical and further discussion is presented follow.

$$L_{eq} = \frac{V_M V_L}{2\pi f_s n P_o}\varphi_{nom}\left(1 - \frac{|\varphi_{nom}|}{\pi}\right) \tag{4}$$

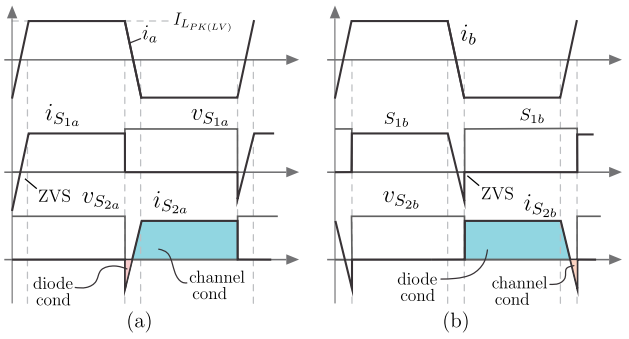

Figure 3. Current and voltage waveforms on the LV side semiconductors (i_{S1a}, v_{S1a}, i_{S2a}, v_{S2a}) and MV semiconductors (i_{S1b}, v_{S1b}, i_{S2b}, v_{S2b}) of the QAB converter. Diode and channel refer to the power device (MOSFET and/or IGBT).

The voltage and current waveforms on the semiconductors of the MV side bridge and LV bridge of the QAB converter are depicted in Fig. 3. If properly designed, the current and voltage waveforms on the semiconductors will be same as depicted in Fig. 3. In this figure, the peak current on the LV side inductor ($I_{L_{PK(LV)}}$) is calculated by (5).

$$I_{L_{PK(LV)}} = \frac{V_L - \sqrt{V_L^2 - 8L_{eq}f_s n V_L I_o}}{4L_{eq}f_s} \tag{5}$$

$$i_{S1a,rms} = \sqrt{\frac{1}{T_s}\int_0^{T_s} {i_{S1a}}^2(t)\,dt} \tag{6}$$

$$i_{S1a,avg} = \frac{1}{T_s}\int_0^{T_s} i_{S1a}(t)\,dt \tag{7}$$

Fig. 4 (a) shows the variation of the peak current on the LV and MV side inductors, according to the nominal phase shift angle chosen on the design, while the Fig. 4 (b) shows the variation of the same current in function of the load for different designed φ. As can be noticed, higher φ implies in higher peak current, and consequently rms current and losses on the semiconductors, inductors and transformer. It means, more reactive power flowing on the converter [10]. Then, a range between 30° to 50° is desired and in this work $\varphi_{nom} = 35°$ is selected.

To calculate the current effort and consequently the losses on the semiconductors and transformer the equations (6) and (7) are used, considering the current waveforms presented in Fig. 3 and positive power flow, i.e. from MV to LV side. As a result, the average and rms current on the semiconductor of the MV cell are calculated by (8) to (11).

$$i_{D_{1b(avg)}} = \frac{I_{L_{PK(LV)}}}{3n}\frac{\varphi}{8\pi} \tag{8}$$

$$i_{D_{1b(rms)}} = \frac{I_{L_{PK(LV)}}}{3n}\sqrt{\frac{\varphi}{12\pi}} \tag{9}$$

$$i_{S_{1b(avg)}} = \frac{I_{L_{PK(LV)}}}{6n}\left(1 - \frac{3\varphi}{4\pi}\right) \tag{10}$$

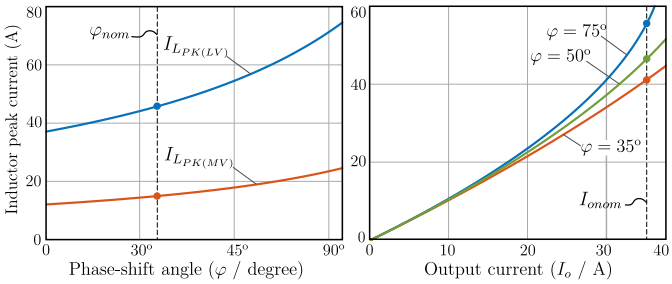

Figure 4. The peak current on the LV inductor and MV inductor in function of the nominal designed phase-shift angle and (b) the same current in function of the output current, for different designed phase-shift angle.

$$i_{S_{1b(rms)}} = \frac{I_{L_{PK(LV)}}}{3n}\sqrt{\frac{1}{2}\left(1 - \frac{5\varphi}{12\pi}\right)} \tag{11}$$

Similarly, the average and rms currents on the semiconductor of the LV cell are calculated by (12) to (15).

$$i_{D_{1a(avg)}} = \frac{I_{L_{PK(LV)}}}{2}\left(1 - \frac{3\varphi}{4\pi}\right) \tag{12}$$

$$i_{D_{1a(rms)}} = I_{L_{PK(LV)}}\sqrt{\frac{1}{2}\left(1 - \frac{5\varphi}{12\pi}\right)} \tag{13}$$

$$i_{S_{1a(avg)}} = I_{L_{PK(LV)}}\frac{\varphi}{8\pi} \tag{14}$$

$$i_{S_{1a(rms)}} = I_{L_{PK(LV)}}\sqrt{\frac{\varphi}{12\pi}} \tag{15}$$

The rms current on the MV and LV inductors are calculated by

$$i_{L_{1a(rms)}} = I_{L_{PK(LV)}}\sqrt{1 - \frac{2\varphi}{3\pi}} \tag{16}$$

$$i_{L_{1b(rms)}} = \frac{I_{L_{PK(LV)}}}{3n}\sqrt{1 - \frac{2\varphi}{3\pi}}. \tag{17}$$

Figs. 5 and 6 show the rms and average currents on the semiconductors (intrinsic body diode and channel) and inductors on the LV side and MV side, respectively, in function of the designed φ. The current efforts on the semiconductors and inductors, and consequently losses, increases with φ. Furthermore, when the power flows from the MV to the LV, most of the current flows through the channel of the MV side semiconductors, whereas it flows mostly through the body diode on the LV side. Therefore, it is very important to select a power semiconductor for the LV side with low forward drop voltage for the body diode.

IV. Losses Analysis and Design of the QAB Converter

As mentioned before, the losses in the main components of the QAB must be carefully computed in function of the main converter parameters, with the aim of properly selecting these parameter, minimizing the losses.

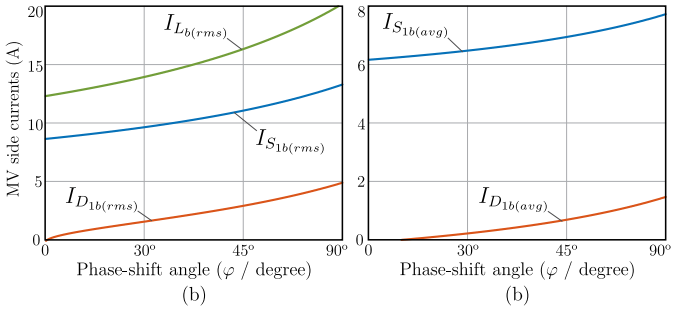

Figure 5. The average and rms currents on the MV side in function of the nominal designed phase-shift angle

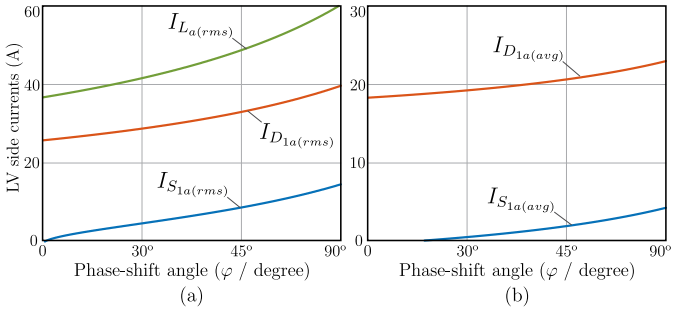

Figure 6. The average and rms currents on the LV side in function of the nominal designed phase-shift angle

A. Semiconductors

An important feature of the modular ST architecture is possibility to use lower blocking voltage semiconductors, implying in a wide variety of device choice during the design. From the converter's specification shown in Table I, 1.2 kV semiconductors can be employed in both sides of the converter, benefiting both efficiency and cost.

In order to take advantage of the high performance of the new SiC devices, SiC-MOSFETs of 1.2 kV voltage rating are considered on the design. These devices are characterized by a very low switching energy and a very low $R_{DS(on)}$. Although the converter is supposed to operate with ZVS, this characteristic is achieved only during the turn-on of the switch, while it turns-off under hard switching. Therefore, by using SiC-MOSFETs, the QAB converter will not only take the advantage of their low $R_{DS(on)}$, reducing the conduction losses considerably, but also the low switching energy, reducing the turn-off losses. Besides that, standard Si-IGBT of 1.2 kV are also taken into consideration during the converter's design, in order to compare the performance of the different devices technologies in this application. The list of the considered semiconductors is presented in Table II. As can be noticed, three different SiC-MOSFETs devices and three different Si-IGBTs are considered on the design. Since different devices can be used on the LV and MV sides, it results in 36 combinations and then 36 designs iterations.

The conduction losses of the MOSFETs can be calculated by (18), where the on-resistance ($R_{ds(on)}$) is function of the drain-source current (i_{ds}), junction temperature (T_J) and gate voltage (V_{gs}). Assuming a constant junction temperature of $100°C$ and a constant gate voltage, the equation is simplified to (19). Similarly, the conduction losses on the diode and IGBT are calculated by (20), where V_f is the forward drop voltage (for diode case) or collector-emitter voltage (for IGBT case), while i_f is the current that flows on the device. The equation can also be simplified to (21).

Table II
SPECIFICATION OF THE SEMICONDUCTORS CONSIDERED IN THE DESIGN

SiC-MOSFET / 1.2 kV					
Name	Reference	I	$R_{ds(on)(@150C)}$	V_F	E_{off}
SIC-2	C2M0040120D	30 A	$84m\Omega$	3.3 V	0.3 mJ
SIC-2	C2M0040120D	40 A	$84m\Omega$	3.3 V	0.3 mJ
SIC-3	C2M0025120D	90 A	$43m\Omega$	3.3 V	0.3 mJ
Si-IGBT / 1.2 kV					
Name	Reference	I	$V_{CE(on)(@150C)}$	V_F	E_{off}
IGBT-1	IHW40N120R3	40 A	$2.4V$	1.3 V	3.1 mJ
IGBT-2	IHW40N120R3	40 A	$1.9V$	1.3 V	3.1 mJ
IGBT-3	IHW40N120R3	40 A	$2.4V$	1.3 V	2.03 mJ

$$P_{MOS(cond)} = \frac{1}{T}\int_0^T R_{ds(on)}\left(i_{ds}(t), T_J, V_{gs}\right)\cdot {i_{ds}}^2(t)\,dt \tag{18}$$

$$P_{MOS(cond)} = R_{ds(on)}\cdot I^2_{S_1(rms)} \tag{19}$$

$$P_{IGBT(cond)} = \frac{1}{T}\int_0^T V_f\left(i_f(t), T_J, V_{gs}\right)\cdot i_f(t)\,dt \tag{20}$$

$$P_{IGBT(cond)} = V_f\cdot I_{f(avg)} + R_f\cdot I^2_{f(rms)} \tag{21}$$

The switching losses can be generally calculated by (22), where $N_{sw(on)}$ and $N_{sw(off)}$ are the number of turn-on and turn-off commutations, respectively, during the time interval T_s. R_g is the gate resistance. As the converter switches always with a constant voltage and it is assumed a constant temperature junction, as well as the V_{gs} and R_g. Because of the ZVS operation, the turn-on losses are neglected, and a simplified equation can be written as presented in (23). The equation as is written in (22) is suitable for a computer implementation, because it is already discretized.

$$P_{(sw)} = \frac{1}{T}\left(\begin{array}{l}\sum_{n=1}^{N_{sw(on)}} E_{on}\left(V_{ce}, I_d, T_J, V_{gs}, R_g\right) + \\ \sum_{n=1}^{N_{sw(off)}} E_{off}\left(V_{ce}, I_d, T_J, V_{gs}, R_g\right)\end{array}\right) \tag{22}$$

$$P_{(sw)} = \frac{1}{T}\left(\sum_{n=1}^{N_{sw(off)}} E_{off}\left(I_d\right)\right) = E_{off}\cdot f_s \tag{23}$$

Replacing the equations (11) to (15) in (19) and using the parameters of Table II, the conduction losses are calculated. Likewise, the switching losses are calculated using the parameters of Tables I and II in equation (23).

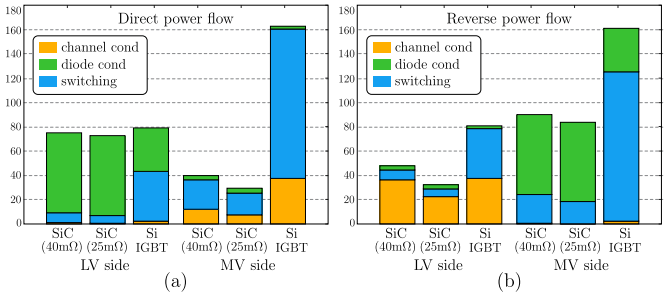

Figure 7. Power dissipation on different semiconductors for the MV and LV side of the QAB converter, for both (direct (a) and reverse (b)) power flow direction.

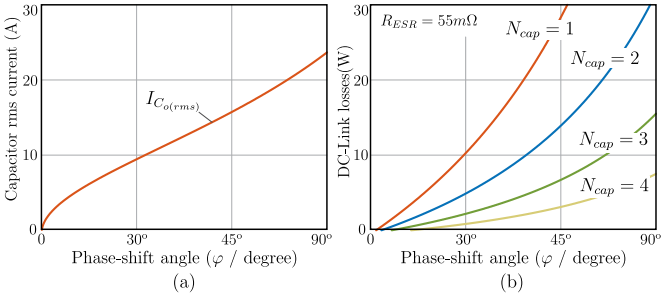

Figure 8. (a) Rms current on the output dc-link capacitor bank, (b) power dissipated on the capacitors dc-link, according to number of parallel capacitors.

A computer-aided algorithm is used to calculate the semiconductors losses and further details are given in the next section. To verify the losses distribution and performance for different technologies, three devices were selected (SiC-2, SiC-3 and IGBT-1) and their losses are calculated for direct and reverse power flow; the result is illustrated in Fig. 7.

Despite of the soft-switching turn-on, the turn-off losses of the QAB are very relevant, mainly when IGBT are employed, because of the high switching energy compared to the SiC-MOSFETS. When the SiC-MOSFET is employed, the current flows through the channel of the LV side semiconductors, instead the body diode, because the gate signal is applied, providing a lower impedance path to the current. Consequently, the losses are reduced even further when compared to the Si-IGBT. For these reason, the diode losses on the SiC-MOSFETs devices are not relevant in Fig. 7. As expected, the performance of the QAB converter is superior when the SiC-3 is used in both sides, regardless the power flow direction.

B. Output DC-Link Capacitor

The rms current through the output capacitor is calculated by (24).

$$I_{C_{o(rms)}} = \sqrt{{I_{L_{PK(LV)}}}^2 \left(1 - \frac{2\varphi}{3\pi}\right) - \left(\frac{V_L}{R_{load}}\right)^2} \qquad (24)$$

For the dc-link capacitor, the aluminum electrolytic capacitor from EPCOS (*long-life* series), with $1000\mu F$ capacitance and voltage rating of 450 V is used. This type of capacitor is chosen because of its high energy storage density. The capacitor has an equivalent-series resistance of $R_{ESR} = 55m\Omega$. Because of the voltage rating of the capacitors, two devices needs to be connected in series. The losses on this component are calculated according to

$$P_{C_o} = 2 \cdot R_{ESR} \cdot I^2_{C_o(rms)}. \qquad (25)$$

The rms current on the output dc-link in function of the designed φ and also the losses on the LV dc-link capacitor in function of the designed φ for different number of parallel capacitors are illustrated in Fig. 8. Parallel capacitors are considered to reduce the current effort, losses and also to provide a relatively high energy storage on the dc-link, guaranteeing the decoupling between both ac sides.

Table III
TRANSFORMER SPECIFICATION USED FOR ITS IMPLEMENTATION

Losses		
Mag inductance	Wire losses	Core losses
$3.2mH$	84 W	60 W
Implemented HFT		
Winding	Leakage inductance	Resistances
LV	$40.7\mu H$	0.08Ω
MV 1	$16.5\mu H$	0.072Ω
MV 2	$13.5\mu H$	0.059Ω
MV 3	$15\mu H$	0.065Ω
Implemented HFT		
Core	3 parallel cores - E 80/38/20	
N° of turns (LV)	$n_{LV} = 24$	
N° of turns (MV)	$n_{MV} = 24$	
wires - (LV)	2000 x AWG44	
wires - (MV)	90 x AWG32	

C. HFT Design

To design the HFT, different core shapes were considered, such as the UU-93 and the EE-80 with ferrite core material N87 from TDK/EPCOS. An algorithm was developed to assist the HFT design. In this algorithm, the basic design is performed according to [18], where the number of turns is calculated, wires are selected and so on. The feasibility of implementation is verified by the window utilization factor. If the transformer can not be built (i.e. the transformer window area is smaller than the required one), then an extra core is considered in parallel to increase the length of the central area, increasing also the magnetic flux allowed in the design. Otherwise, the algorithm goes to the next point: losses calculation. For the wire losses, the skin and proximity effect are considered additionally to the dc losses. To avoid the skin effect, litz wire is used. To losses caused by proximity effect are estimated based on [19]. For the core losses, the generalized Steinmetz equation [20] is used.

The design result is summarized in Table III. As can be noticed, three cores type E 80/38/20 were used in parallel. Detail of the implementation is also presented in Table III. In order to validate the design and obtain the losses, the transformer was built and characterized in laboratory, where the main parameters and losses were measured. The results are presented in Table III.

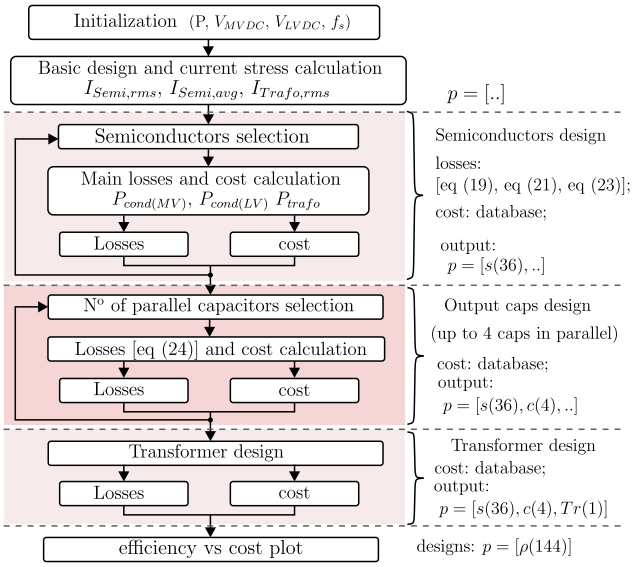

Figure 9. Flowchart of the implemented algorithm used for the QAB design.

D. Final Converter Design

In order to find a optimum trade-off between efficiency and cost of the QAB converter, a computer-aided based design was used and the flowchart of the developed algorithm is shown in Fig. 9. The precise cost estimation is more difficult to be obtained, because it is highly dependent on the market parameters, that can change the price over the time, like: distributor, quantity acquired, etc. As a matter of comparison, the cost used in this algorithm for the semiconductors were obtained directly from the devices manufactures, i.e. *Infineon Technology* [21] for the Si-IGBT and *Cree Wolfspeed* for SiC-MOSFET [22]. For the capacitor and transformer cost, the cost were obtained through the well-known distributor Mouser Electronics [23].

The algorithm starts with the basic design of the converter, as shown in Section III, where the converter's parameters are calculated, like: required inductance, phase-shift angle, current efforts, etc. Then, it selects the semiconductors and calculate their losses and cost. At this point, there is an iteration to calculate the losses and cost for all possible combination of semiconductors. The next point is the output capacitance selection, where an iteration is performed to find the proper number of parallel capacitors according to cost and losses. Finally, the HFT is designed, as described in the previous section.

As a result, the theoretical efficiency of the QAB versus its cost for several designs performed by the algorithm is plotted in Fig. 10. Three designs are highlighted in this figure: (1) lowest cost and lowest efficiency; (2) best trade-off between cost and efficiency; (3) highest efficiency and highest cost. The semiconductor selected in each of the pointed-out designs is shown in Fig. 10, as well. As can be noticed, the lowest cost and efficiency is obtained when IGBT are employed in both side of the QAB converter. The device SiC-3 provides the best

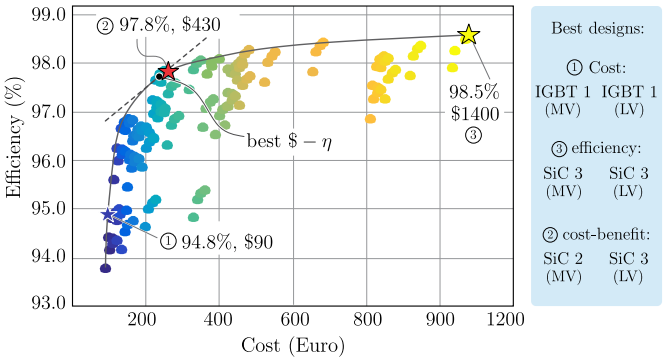

Figure 10. Theoretical efficiency of the QAB versus its cost for different designs.

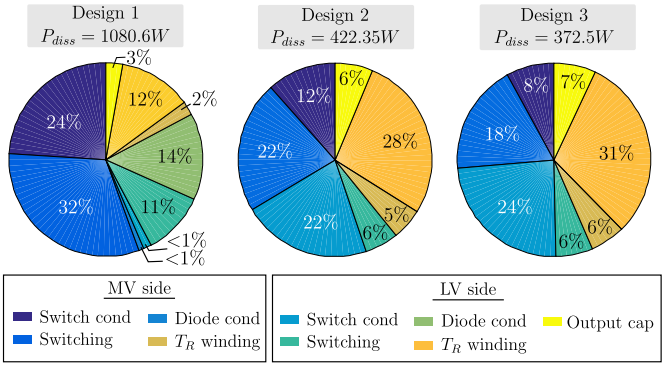

Figure 11. Losses distribution on the main devices for the three designs highlighted: (a) lowest cost, (b) best cost-efficiency trade-off, (c) highest efficiency.

performance, because it has the lowest $R_{DS(on)}$, i.e. conduction losses, and switching losses. However, it is the most expensive solution. When SiC-2 is used in the MV and SiC-3 on the LV side of the QAB, the efficiency decreases slightly, but the cost decreases significantly. Therefore, this design presents the best trade-off between cost and efficiency. The losses distribution on the components of the QAB converter for the three highlighted design are shown in Fig. 11. As can be reinforced, even operating with ZVS during the turn-on, the power dissipated during the turn-off is very relevant,

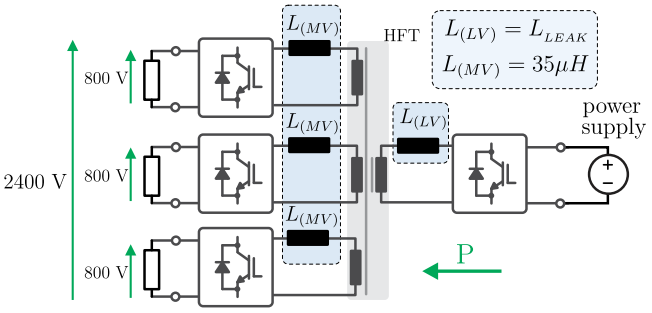

Figure 12. Scheme of the tested prototype, presenting its connection to the load and the external transformer implementation.

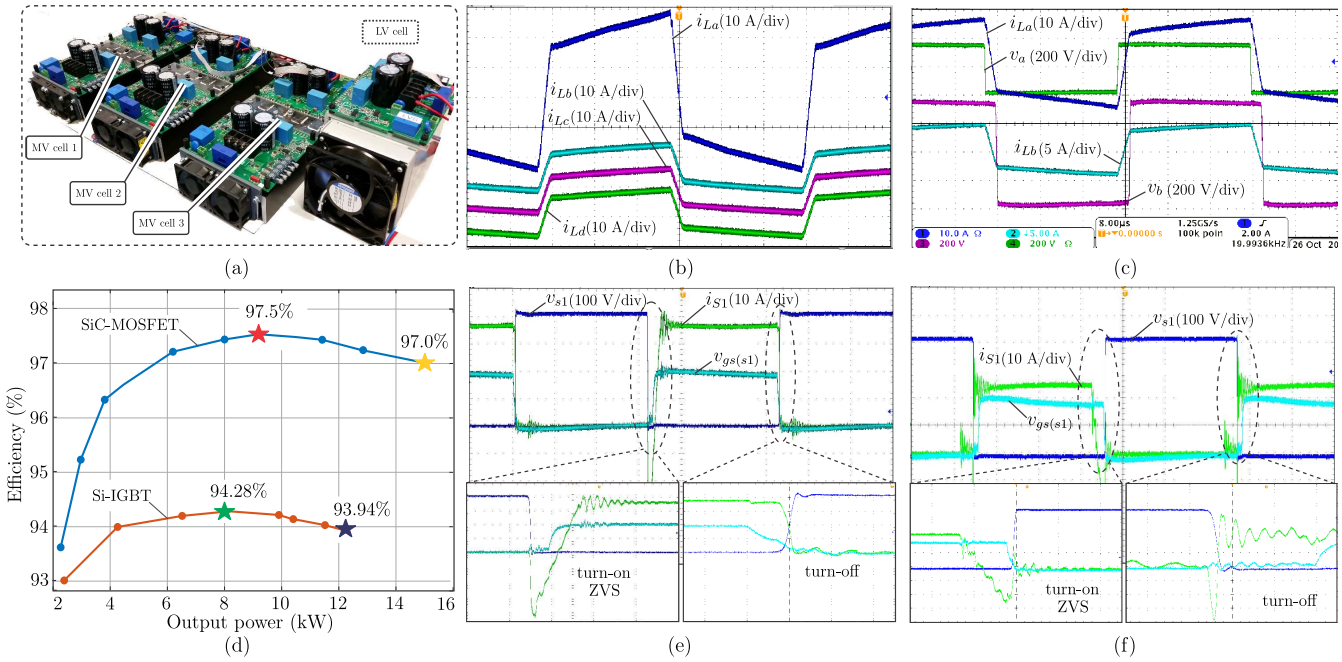

Figure 13. Experimental results of the implemented ST prototype: (a) picture of the implemented prototype, (b) inductor current waveforms on the LV side (i_{La}) and MV side (i_{Lb}, i_{Lc} and i_{Ld}) of the QAB converter, (c) main voltage and current waveforms on the LV side (v_{La}, i_{La}) and MV side of the QAB (v_{Lb}, i_{Lb}) converter, (d) efficiency curve in function of the output power of the converter, (e) commutation of the LV side semiconductor (s_{1a}) and (f)commutation of the MV side semiconductor (s_{1b}).

when IGBT is used. Therefore, it is very advantageous and recommended to use SiC-MOSFETs in this converter.

V. Prototype Implementation and Experimental Results

In order to evaluate the converter performance experimentally and verify the presented design procedure, a prototype was built and tested. The main specifications are shown in Table I. The details about the converter construction and the final results are discussed.

A. Final Prototype Assembly

From the previous design methodology, the QAB converter presents the best cost for the design 1 and the best cost-benefits for the design 2, (see Fig. 10). Therefore, both combination are used on the construction and test of the prototype, in order to evaluate experimentally the benefits to use SiC.

The imperfect construction of the transformer causes a deviation of the leakage inductance values of the MV side windings ,i.e. $L_{b_{leak}} \neq L_{c_{leak}} \neq L_{D_{leak}}$. To reduce this effect, external inductor should be used on the MV side, resulting in $L_{(b,c,d)} = L_{(b,c,d)_{leak}} + L_{ext}$. To reach the desired inductance value of $75\mu H$ seen by the LV side, three additional inductors of $35\mu H$ are used in MV side (resulting in $35\mu H/3 = 11.6\mu H$ seen by the LV side). These additional inductors associated to the leakage inductance of the HFT result in the desired inductance value.

Fig. 12 shows the block diagram of the schematic used to test the converter. For simplicity's sake, the converter was tested with reverse power flow, where a single dc power supply was used on the LV side and three loads were connected on the MV side. Fig. 13 (a) shows the picture of the prototype, where the cells of the CHB associated to the QAB converter (see Fig. 1) is observed, sharing the same cooling system.

B. Experimental Results

The experimental results were obtained for the converter operating in steady-state with balanced power, i.e. equal power processed by the MV cells, where the main waveforms were saved. Additionally, the efficiency curve of the QAB is obtained and discussed, when Si-IGBT (design 1) and SiC-MOSFETs (design 2) are used. The results are summarized in Fig. 13.

Fig. 13 (b) shows the main waveforms of the converter operating in steady-state, where the currents on the LV cell (i_{La}) and MV cells (i_{Lb}, i_{Lc}, i_{Ld}) are presented. From this result, the balanced operation of the QAB converter is noticed, where each MV cell process the same amount of power. Similarly, Fig. 13 (c) shows voltage and current on the ac side of the MV bridge (v_{Lb} and i_{Lb}) and LV bridge (v_{La} and i_{La}), where the phase shift operation of these bridges is observed. These waveforms are in accordance with the theoretical one shown in Fig. 2. The commutation of the switches for the LV and MV sides is presented in Fig. 13 (e) and (f). Fig. 13 (e) shows the current and voltage on the LV side semiconductor (s_{1a}), as well as the commutation detail, where soft-switching operation is verified. As expected, the semiconductor turns on in ZVS and turns off under hard-switching. However, the

constant current imposed by the inductance during the dead-time of the switches discharges the output capacitance of the switch (s_{1a}), while charges the capacitance of the respective switch of the leg, (i.e. s_{2a}), implying in a commutation losses reduction (almost ZVS operation). This features is obtained only when SiC-MOSFETs are used. Likewise, the current and voltage on the MV side semiconductor (s_{1b}) is illustrated in 13 (e), as well as the commutation details. The same effect described for s_{1a} is also observed in the MV side switch s_{1b}.

Finally, the efficiency curve in function of the output power is shown in Fig. 13 (d). The efficiency curve was obtained experimentally using the high performance power analyzer WT1800 from Yokogawa (basic power accuracy of 0.02%). As can be seen, the converter has achieved a peak efficiency of 94.28% at a power level of around 8 kW, when IGBT are used (design 1), while at nominal load the converter has achieved around 93.4% of efficiency. For the design 3, where SiC-MOSFETs are used, the converter has achieved a peak efficiency of 97.5% at a power level of around 8.5 kW and its efficiency is 97% at nominal load. Therefore, the use of SiC-MOSFETs results in a losses reduction of 57% at 8 kW (increasing the efficiency in 3.3%) and a losses reduction of 56.1% at 12 kW (increasing the efficiency in 3%). These results confirmed the optimum design of the converter, as well as the high potentiality of the SiC technology in this application.

VI. Conclusion

In this paper, the quadruple active bridge is used as a basic building block to implement a modular smart transformer. Since the efficiency and cost are very important in this application, a multi-objective optimization algorithm was developed. The losses on the components were modeled and a database with the cost and electric characteristics of each component was created. The algorithm combines these parameters in order to find the optimum point for cost, efficiency and the best trade-off between cost and efficiency. Besides that, SiC-MOSFETs and Si-IGBT were considered on the design of the converter. From these design, a 20 kW prototype was build and tested. The experimental results have shown an efficiency of 97.5%, which is the highest obtained so far for this kind of converter. It demonstrates the effectiveness of the proposed design. Regarding the converter's performance with different semiconductors technology, it was verified that the SiC-MOSFETs is more advantageous, due to its low energy losses, almost ZVS operation (during the switch turn-off) and the conduction of the reverse current through the channel, instead the diode, reducing the conduction losses. Consequently, the use of SiC-MOSFETs reduced the converter's losses in around 57%, compared to the IGBT. These results demonstrate the feasibility of this technology is such application.

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