Solid-State Transformer Architecture Using AC–AC Dual-Active-Bridge Converter

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***Abstract*—Modern development of semiconductor power-switching devices has promoted the use of power electronic converters as power transformers at the distribution level. This paper presents an ac–ac dual-active-bridge (DAB) converter for a solid-state transformer. The proposed converter topology consists of two active H-bridges and one high-frequency transformer. Four-quadrant switch cells are used to allow bidirectional power flow. Because power is controlled by the phase shift between two bridges, output voltage can be regulated when input voltage changes. This paper analyzes the steady-state operation and the range of zero-voltage switching. It develops a switch commutation scheme for the ac–ac DAB converters. Experimental results from a scaled-down prototype are provided to verify the theoretical analysis.**

***Index Terms*—Bidirectional ac–ac converter, dual-active-bridge (DAB) converter, phase-shift modulation (PSM), solid-state transformer (SST), zero-voltage switching (ZVS).**

I. Introduction

With the rapid development of power-switching devices, it is becoming possible to apply high-frequency pulsewidth modulation (PWM) converters as solid-state transformers (SSTs) at the distribution level [1]–[6]. An SST is, in essence, an ac–ac switching power converter with medium-voltage input (such as 7.2 kV) and low-voltage output (such as 240 V). SSTs are among the key components in the Future Renewable Electric Energy Delivery and Management System [7], a prototype for next-generation power systems with high penetration of energy storage and generation at the distribution level. SSTs use less copper, which is increasingly expensive, and more semiconductor devices, which are increasingly inexpensive. The cost of SSTs will become more economical as semiconductor technology advances. Furthermore, SSTs provide more values for distribution systems, such as power flow control and protection against voltage sag and swell [7], [8]. With the advent of reliable high-voltage devices based on silicon carbide (SiC) [9], [10], SSTs are nearing commercial feasibility [11]. Controllable SiC devices, such as JFETs or insulated-gate bipolar transistors (IGBTs), enable operation at higher voltage with fewer series-connected devices and/or phases. The conventional approach is to use an input-series–output-parallel topology, similar to that in [12], to achieve the necessary input-voltage and output-current ratings [2], [13]. For example, the proposed topology could achieve 7.2-kV–240-V conversion using two input-series–output-parallel-connected phases using 10-kV SiC devices on the high-voltage side and 600-V Si devices on the low-voltage side.

Several power converter topologies have been proposed for single-phase SSTs. Multistage ac–dc–ac–dc–ac SST schemes were introduced in [1], [2]. These approaches use cascaded connections of active front-end rectifiers, isolated dc–dc converters, and load-side inverters. They provide maximum functionality and control flexibility, but they have complex circuit configurations, large number of passive components, and low power efficiency [14]. On the other hand, the methods in [4], [5], [15], and [16] have applied a single-stage direct ac–ac power conversion scheme to SSTs. Fewer conversion stages reduce circuit complexity and increase reliability. However, the topologies in [4] and [5] do not use soft switching, and those in [15] and [16] do not have a symmetrical circuit structure to facilitate bidirectional power flow. The works in [17]–[21] presented other topologies of direct ac–ac power conversion; however, neither topology provides the galvanic isolation necessary for a distribution transformer. A two-stage SST could be constructed using the ac–dc isolated converter of Martin *et al.* [22] and Casarin *et al.* [23], which has some aspects in common with the proposed topology despite its dc output. The proposed topology reduces the number of stages (to a single stage), provides galvanic isolation, and enables regulation of power flow, voltage magnitude, and harmonic content.

The dc–dc dual-active-bridge (DAB) converter was introduced in [24]–[26] for high-power applications. DC–DC DAB converters have been used in electric automobiles [27], ultracapacitor systems [28], photovoltaic systems [29], and power systems [30]. Recent advancement in dc–dc DAB converters includes new modulation methods [31], new topology using a novel soft-switching technique [32], detailed models [33]–[35], optimization for efficiency [36], [37], and closed-loop control [38], [39]. DC–DC DAB converters can be used for the middle section of a multistage SST [2].

Direct ac–ac DAB converters were proposed for SST applications by the authors in [3]. Although superficially similar to the direct ac–ac converter in [5], the proposed ac–ac DAB converter incorporates significant leakage inductance in the high-frequency transformer. Therefore, the proposed topology is capable of output-voltage regulation via phase-shift modulation (PSM) and also has a wide soft-switching range for higher efficiency. Because of simple circuit configuration and soft switching, the proposed topology has higher efficiency

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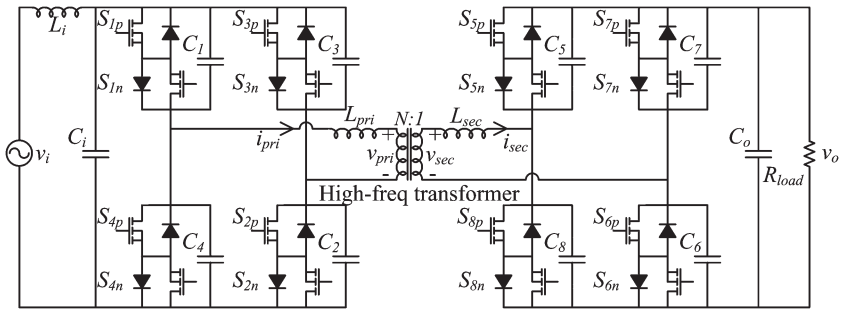

Fig. 1. DAB converter schematic.

than multistage topologies, as discussed in Section IV [14]. The topology is capable of regulating the magnitude of the secondary-side voltage to be fixed, regardless of the primary-side voltage. Also, the presence of leakage inductance limits the di/dt at short-circuit conditions, which helps short-circuit protection. This paper extends the discussions in [3], stressing the effect of introducing ac–ac power conversion. Furthermore, it presents the design and test results of a scaled-down ac–ac DAB converter prototype.

In Section II, conventional dc–dc DAB analysis is adapted to the ac–ac case, including an analysis of load power factor and its effect on soft switching. In Section III, a new switch commutation scheme is presented, which is needed because of the antiserial connection of unidirectional switches in each ideal switch location (see Fig. 1). The same switching pattern holds for both hard and soft switching. Section IV briefly discusses the efficiency advantage of the proposed topology over other SST types. Section V describes an experimental ac–ac DAB rated for 220-V input, 120-V output, 60 Hz. Soft switching and voltage regulation are verified. Section VI concludes with a discussion of challenges that affect this and other SST topologies.

II. Analysis of AC–AC DAB Converters

The proposed ac–ac DAB converters have a symmetric configuration, which consists of two H-bridges, each fed by a voltage source, and one high-frequency transformer. The high-frequency transformer provides both galvanic isolation and energy storage in its winding leakage inductance. Whereas a previous topology [5] requires leakage inductance that approaches zero, the proposed topology uses the nonzero leakage to facilitate voltage regulation and soft switching. The soft-switching ac–dc topology of Martin *et al.* [22] and Casarin *et al.* [23] also resembles the proposed topology but requires a current source on one terminal.

Two antiserial-connected switching devices form one switch cell to block ac voltage and conduct ac current. A resonant capacitor in parallel with each switch cell enables soft switching. Fig. 1 shows the circuit configuration of an ac–ac DAB converter. Note that IGBTs can be used in place of power MOSFETs. An ac–ac DAB converter is controlled by PSM. Power flows from the leading bridge to the lagging bridge. The inherent symmetry of the power circuit in an ac–ac DAB converter ensures bidirectional power flow.

The work in [3] derived a per-unit model to analyze the steady-state operation of an ac–ac DAB converter. By using the per-unit model, the parameters of an SST's both sides can be scaled easily to design a voltage step-up/down SST. When a per-unit system at both sides of an SST is defined, the input voltage v_i, output voltage v_o, primary-side transformer current $i_{\rm pri}$, and secondary-side transformer current $i_{\rm sec}$ of an ac–ac DAB converter are converted to their per-unit variables $v_{i,\rm pu}$, $v_{o,\rm pu}$, $i_{\rm pri,pu}$, and $i_{\rm sec,pu}$, respectively. Note that $i_{\rm pri,pu} = i_{\rm sec,pu} = i_{\rm pu}$.

The switching frequency is much higher than the grid frequency, which means that the same quasi-steady analysis method of average transformer current can be applied. According to Qin and Kimball [3], the amount of power transferred to the load is controlled by the phase-shift angle ϕ between two bridges

$$P_o = \frac{v_{i,\rm pu} v_{o,\rm pu}}{X_{\rm pu}} \left(\phi - \frac{\phi^2}{\pi}\right) \tag{1}$$

where $X_{\rm pu}$ is the lumped transformer leakage reactance in per unit and ϕ is in radians. Using per-unit notation, the ideal dc voltage transfer ratio is

$$\gamma = \frac{v_{o,\rm pu}}{v_{i,\rm pu}} = \frac{R_{\rm pu}}{X_{\rm pu}} \phi \left(1 - \frac{\phi}{\pi}\right) \tag{2}$$

where $R_{\rm pu}$ is the per-unit load resistance. However, (2) does not hold for the ac–ac case when there exists an output filter. Given base power S_b and base secondary-side voltage $V_{\rm sec}$, base secondary-side impedance can be defined as $Z_{b,\rm sec} = S_b / V_{b,\rm sec}$. In the steady state of an ac system, (1) becomes

$$P_i = v_{i,\rm pu} \hat{i}_{i,\rm pu} = P_o = \frac{v_{o,\rm pu}^2}{R_{\rm pu}} + \frac{d}{dt}\left(\frac{1}{2} C_{\rm pu} v_{o,\rm pu}^2\right) \tag{3}$$

where $C_{\rm pu} = C_o \cdot Z_{b,\rm sec}$ and C_o is the output filter capacitance. By converting (3) into the frequency domain, the voltage transfer ratio becomes

$$\gamma_{\rm ac} = \frac{1}{X_{\rm pu}} \phi \left(1 - \frac{\phi}{\pi}\right) \frac{R_{\rm pu}}{s R_{\rm pu} C_{\rm pu} + 1}. \tag{4}$$

Equation (4) shows that the ac voltage transfer ratio of an ac–ac DAB converter is determined by transformer leakage inductance, phase shift between bridges, output filter, and load resistance. The load and the output filter introduce a small phase shift between input and output voltages in steady state. This steady-state model is valid for frequencies much lower than the switching frequency. According to (4), output voltage will

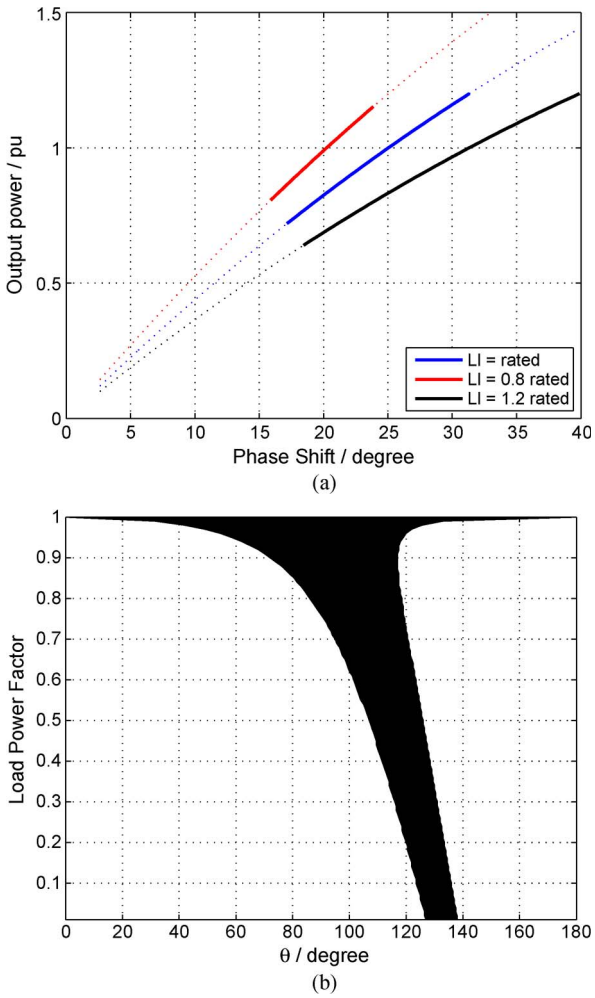

Fig. 2. Soft-switching analysis. For (a), transfer ratio fixed at 1.0 pu, the rated inductance is given in Table II, and solid lines represent soft-switching range; for (b), transfer ratio fixed at 1.0 pu, leakage inductance is fixed at the designed values in Table II, and shaded area represents soft-switching range. (a) Effect of leakage inductance on soft-switching range. (b) Effect of load power factor on soft-switching range.

vary sinusoidally as input voltage varies. Because ac–ac DAB converters use four-quadrant switching cells, this ratio holds, regardless of the polarity of input voltage and the direction of transformer current. In steady state, output voltage follows input voltage sinusoidally. This confirms the feasibility of applying ac–ac DAB converters as galvanically isolated fixed-frequency SSTs.

The ac–ac DAB topology offers soft switching for all switches, which increases efficiency. The soft-switching range under different load conditions are already presented in [3]. Based on the soft-switching condition in [3, eq. (12)], Fig. 2(a) shows the effect of transformer leakage inductance on soft-switching range. It illustrates whether soft switching is valid when output power varies and voltage transfer ratio is fixed at 1.0 pu. Increasing leakage inductance results in a wider soft-switching range. However, high leakage inductance limits power output capability. Fig. 2(b) shows the effect of load power factor on soft-switching range. In Fig. 2(b), θ means the angle in a 60-Hz sinusoidal cycle of the output voltage. As load power factor decreases, more phase shift between input and output voltages causes a narrower soft-switching range. The soft-switching range of the other half cycle (180°–360°) can be analyzed similarly due to the symmetry of converter topology.

III. Switch Commutation Scheme

The proposed ac–ac DAB converters use four-quadrant switches, which makes switching commutation difficult. Multistep commutation schemes are normally used for hard switching [5] because inductive current should not be open and capacitive voltage should not be shorted. One advantage of the proposed ac–ac DAB converter is that it permits soft switching over a wide range. Inductive current can be conducted through capacitors when no switching device is conducting during soft-switching commutation. This approach makes switch commutation less challenging. However, as discussed in [3], the criteria for zero-voltage switching (ZVS) cannot be met for all operating conditions. Therefore, a method to transition seamlessly between soft and hard switching must be developed. This paper presents a novel switch commutation scheme to permit both soft and hard switching that uses transformer current as a reference signal. Table I summarizes the commutation sequence. Fig. 3 shows that this commutation scheme is suitable for both switching scenarios. The switching commands are the same for switches in a pair, e.g., S_{1p} is the same as S_{2p}, while S_{3n} is the same as S_{4n}.

There are three transient switching states. As shown in Fig. 3(a), before switching commutation, S_{1p}, S_{1n}, S_{2p}, and S_{2n} are conducting. The transformer current is positive enough to satisfiy the conditions for soft switching. At t_0, the nonconducting switches (S_{1n} in this case) are turned off. Since S_{1p} is still conducting, S_{1n} is turned off at zero voltage. The first transient state $(t_0{-}t_1)$ is relatively short, just for the nonconducting switches to turn off. At t_1, the to-be-conducting switches (S_{4n}) in the incoming switching cells are turned on. However, they do not begin conducting because the diode in parallel with S_{4p} is reverse biased. Thus, S_{4n} is turned on at zero current. At t_2, turning off the outgoing switches (S_{1p}) starts the resonating commutation. C_1 is being charged while C_4 is being discharged. No switch conducts during this process, and the dv/dt across switches is limited. After completing the commutation from the outgoing to the incoming switch cells, S_{4p} is turned on at zero voltage at t_3. The switch cells are again ready to conduct bidirectional current, and the converter enters another conducting state. All four switching devices commutate at soft switching.

At the operating point shown in Fig. 3(b), the transformer current is negative before the switching transient, meaning that soft switching is not valid. However, the same commutation scheme can be applied. The commutation process begins with turning off the nonconducting switches at t_0. They turn off at zero voltage. Then, at t_1, the incoming switches are turned on at hard switching. The energy stored in C_4 is also discharged through S_{4p} during t_1–t_2, resulting in an inrush current spike. Because the dv/dt is not controlled, it is a hard-switching event. During this process, C_1 is charged by the source voltage. Once the voltage on C_1 rises, S_{1n} stops conducting because the diode

TABLE I
CURRENT-BASED COMMUTATION

	$i_t > 0$					$i_t < 0$				
	State 1	Transient			State 2	State 1	Transient			State 2
	Before t_0	t_0–t_1	t_1–t_2	t_2–t_3	After t_3	Before t_0	t_0–t_1	t_1–t_2	t_2–t_3	After t_3
S1p	1	1	1	0	0	1	0	0	0	0
S1n	1	0	0	0	0	1	1	1	0	0
S2p	1	1	1	0	0	1	0	0	0	0
S2n	1	0	0	0	0	1	1	1	0	0
S3p	0	0	0	0	1	0	0	1	1	1
S3n	0	0	1	1	1	0	0	0	0	1
S4p	0	0	0	0	1	0	0	1	1	1
S4n	0	0	1	1	1	0	0	0	0	1

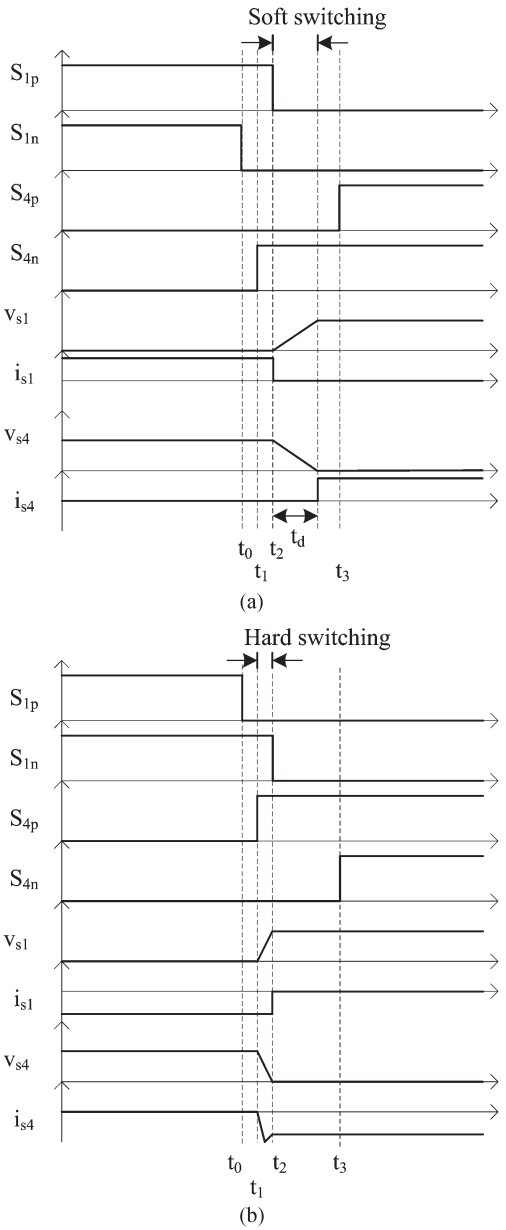

Fig. 3. Switch commutation from S1 to S2. (a) Soft-switching case. (b) Hard-switching case.

is reverse biased. At t_2, the outgoing switches (S_{1n}) are turned off. Moreover, at t_3, S_{4n} turns on. The converter enters another conducting state, and hard-switching commutation ends.

Since a switching device cannot be turned on or off instantaneously in practice, it is necessary to insert deadtime in the commutation scheme described earlier. The time interval from t_0 to t_1 must be long enough to turn off nonconducting switches, and the time interval from t_1 to t_2 must be long enough to turn on incoming switches. Considering device switching specifications and safety margin, the deadtimes t_0–t_1 and t_1–t_2 are both 400 ns in the experimental system described in Section V. Outgoing switches must be turned off after ZVS transients, which means that $t_3 - t_2 > t_d$, where t_d is the amount of time to complete ZVS transients. The dv/dt across the switching device can be approximated by

$$\frac{dv}{dt} = \frac{V}{t_d} = \frac{i_t}{C_r} \tag{5}$$

where V is the voltage across C_i or C_o, i_t is the transformer current during commutation, and C_r is the resonant capacitor. Therefore, the deadtime for ZVS transient is

$$t_d = C_r \frac{V}{i_t}. \tag{6}$$

t_d is a design tradeoff. Switching energy is low if C_r is large. However, large C_r leads to large t_d. In (6), t_d is small if i_t is large, which means that the soft-switching range is limited. However, t_d is too long if a very wide soft-switching range is required. When V varies sinusoidally over a period of 60 Hz, i_t also varies sinusoidally. Therefore, the peak voltage and current can be used. In this paper, soft switching is valid until power is less than 0.3 pu. For instance, at the low-voltage side, the rated output rms voltage is 120 V, and the rated output rms current is 1.2 A. Given a design choice of $C_r = 4.7$ nF, an input voltage of $V = 120$ V, and the load point corresponding to 0.3-pu power is $i_t = 0.3 \times 1.2 = 0.36$ A, $t_d = 1.56$ μs according to (6). Therefore, the deadtime from t_2 to t_3 is chosen to be $t_d = 2$ μs. The deadtime for the high-voltage side is calculated in a similar way.

IV. EFFICIENCY DISCUSSION

A complete analysis of the efficiency of the proposed ac–ac topology was compared to alternative SST topologies in [14]. Fig. 4 shows four potential 20-kVA 7.2-kV/240-V SST configurations using silicon-based power devices. All have power electronic converters that can actively control power flow;

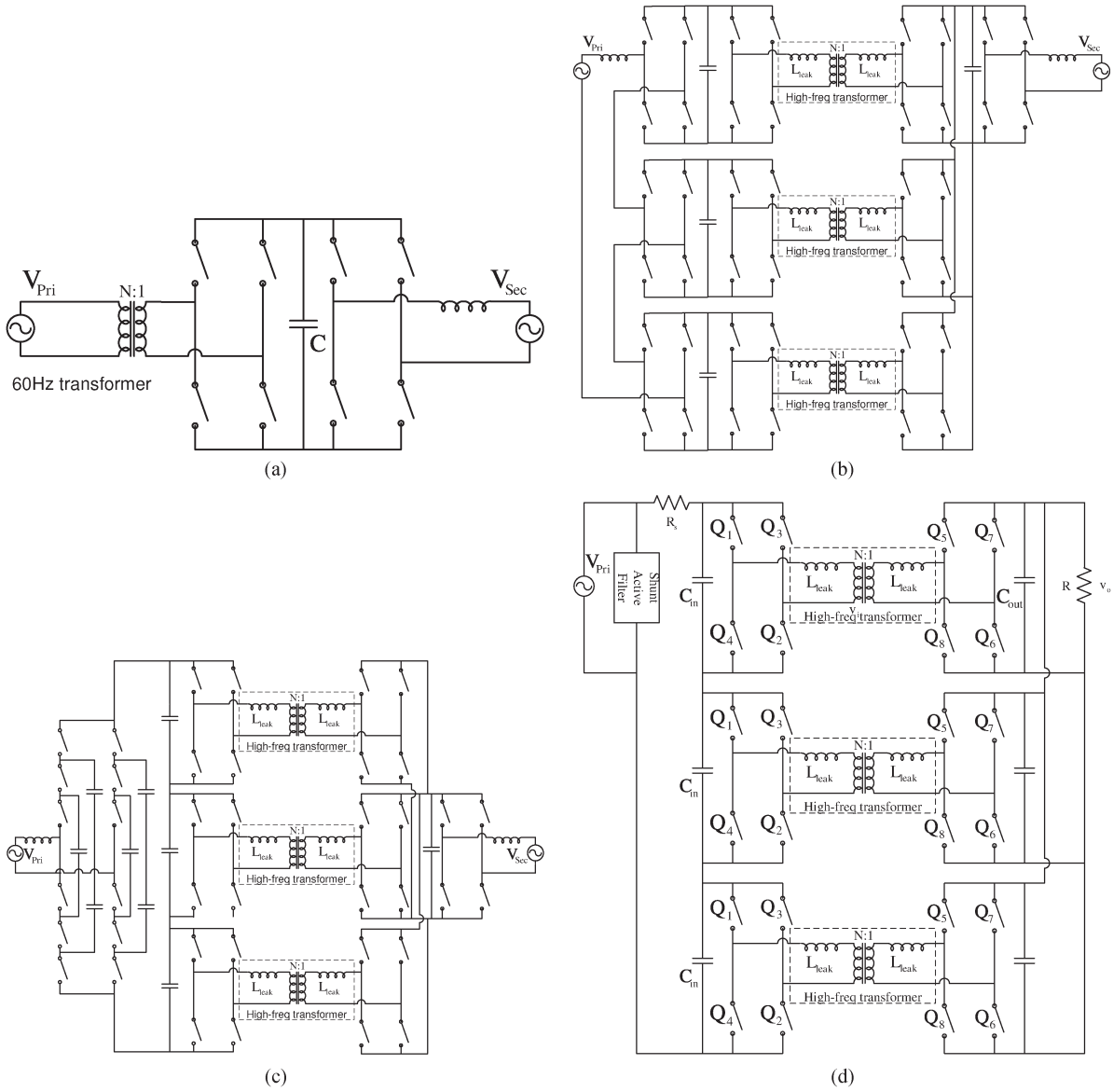

Fig. 4. Four candidate SST topologies. (a) SST1. (b) SST2. (c) SST3. (d) SST4.

therefore, they are categorized as SSTs. These topologies are: 1) a back-to-back voltage source converter with a conventional 60-Hz transformer (SST1); 2) a three-stage SST with a two-level input-series front end (SST2); 3) a three-stage SST with a four-level flying-capacitor front end; and 4) the single-stage ac–ac DAB-converter-based SST in this paper (SST4).

For SST1, SST2, and SST3, the standard implementation uses hard switching in the inverter and rectifier sections. Soft switching may be achieved with the addition of an auxiliary resonant commutated pole (ARCP) in place of each hard-switching pole. The ARCP reduces switching loss but does not improve other losses—in fact, it may increase conduction losses. A loss breakdown is shown in Fig. 5 for each topology, with and without an ARCP, as compared with the new topology (SST4), which does not require an ARCP. In all cases, transformer loss is a significant factor. Topologies SST2 and SST3 include multiple power processing stages, and efficiency suffers accordingly. From an efficiency standpoint, SST1 is the best; however, it requires a 60-Hz transformer, and so does not achieve any of the size benefits. Among those topologies that use a high-frequency transformer, the ac–ac DAB (SST4) is the most efficient. The main drawback of SST4 is the lack of a dc bus for connection of dc loads or sources.

V. Simulations, Hardware Design, and Experimental Results

Simulation results have already been presented in [3]. For ease of comparison to experiments, two simulated steady-state cases are shown in Figs. 6 (transformer voltages and currents near the peak of the sine wave) and Fig. 7 (transformer voltages and currents near the zero crossing of the sine wave). The simulations compare favorably to the experimental results in Figs. 19 and 20.

A simple closed-loop controller, consisting of integral control of the voltage magnitude, was also simulated. The

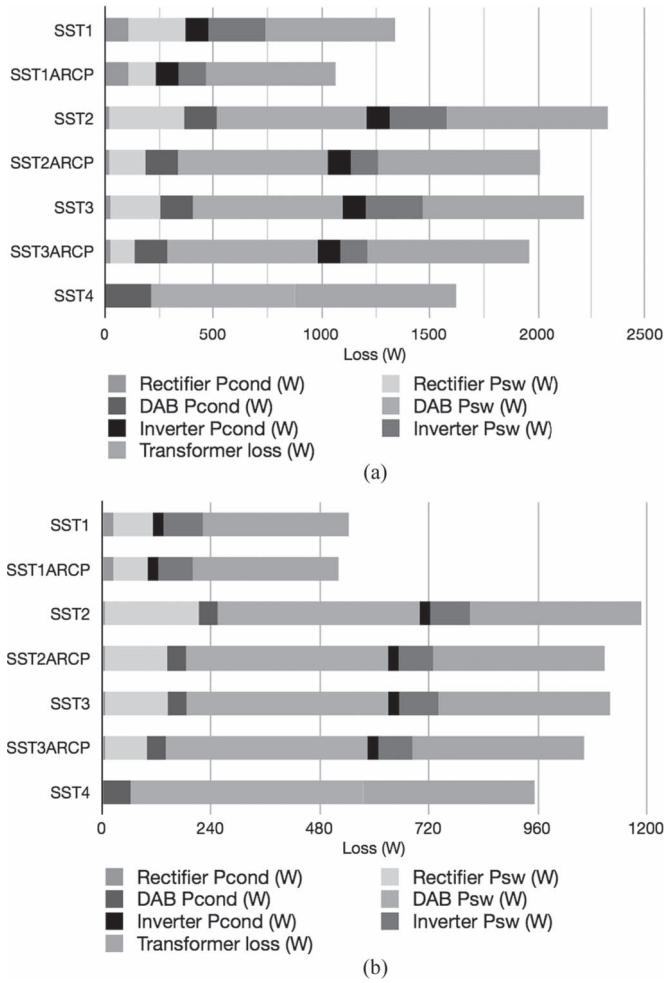

Fig. 5. Loss breakdown (see [14] for more details). (a) Full load. (b) Light load.

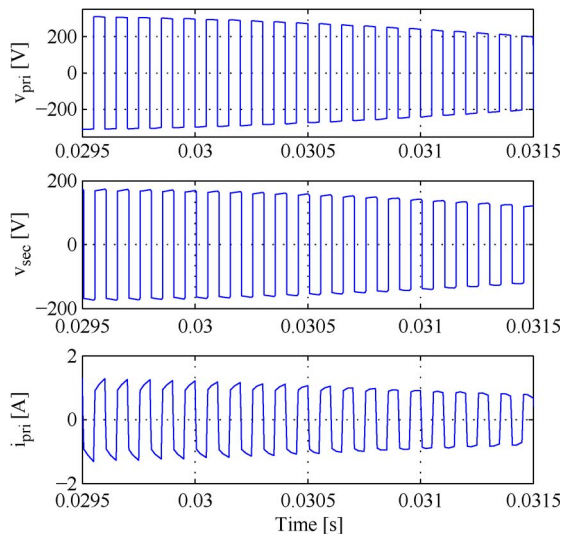

Fig. 6. Simulated transformer voltages and primary current near the peak of the sine wave, with 1.0-pu source and load.

start-up transient and response to a step change in input voltage are shown in Fig. 8. After a brief transient, caused by the 120-Hz zero-order hold implemented here, the output-voltage magnitude remains constant despite an input-voltage change

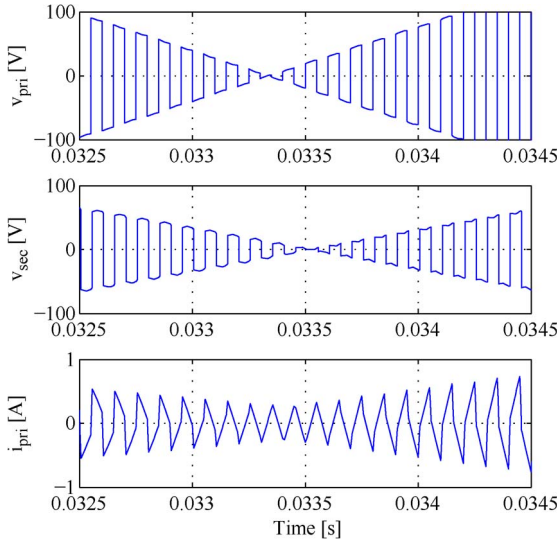

Fig. 7. Simulated transformer voltages and primary current near the zero crossing of the sine wave, with 1.0-pu source and load.

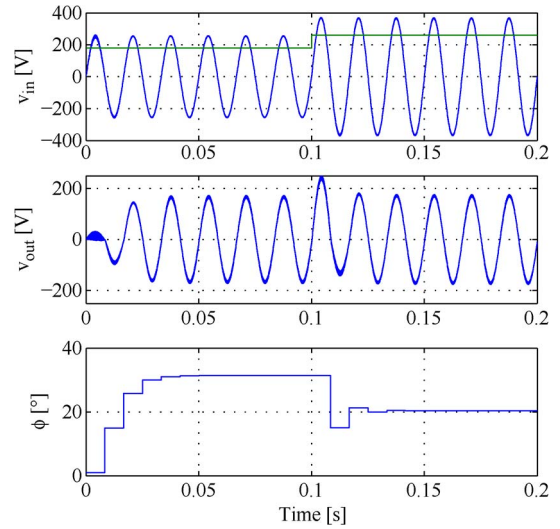

Fig. 8. Simulated closed-loop response to a step change in input voltage. Input-voltage rms magnitude superimposed on $v_{\rm in}$ trace.

TABLE II
CIRCUIT PARAMETERS

Inductance, HV	Inductance, LV	Switch Frequency
900 μH	334 μH	10 kHz
ZVS Capacitor, HV	ZVS Capacitor, LV	Switching Device
2.7 nF	4.7 nF	ST STD8NM60ND 600V 7A MOSFET
Input Capacitor	Output Capacitor	Load Resistor
3 μF	4 μF	100 Ω

from 180 to 260 V that occurs at $t = 0.1$ s. A more sophisticated controller could be implemented using a model similar to the dc–dc case analyzed in [40] and dq modeling as in [41], so that harmonics could be controlled in addition to the rms magnitude.

Two antiseries-connected MOSFETs form one four-quadrant switching cell. Turning both MOSFETs on permits conduction of bidirectional current, as in synchronous rectification. A ferrite core (ETD-49) was used to build the high-frequency transformer. Tables II and III summarize circuit parameters and

TABLE III
TRANSFORMER DESIGN

Core Type	Ferrite ETD49
Core Area	2.11 cm^2
Window Area	2.73 cm^2
wire, HV	120 turns AWG 20
wire, LV	70 turns AWG 20
MMF Layout	HV: 3 portions, 1 layers LV: 2 portions, 1 layer

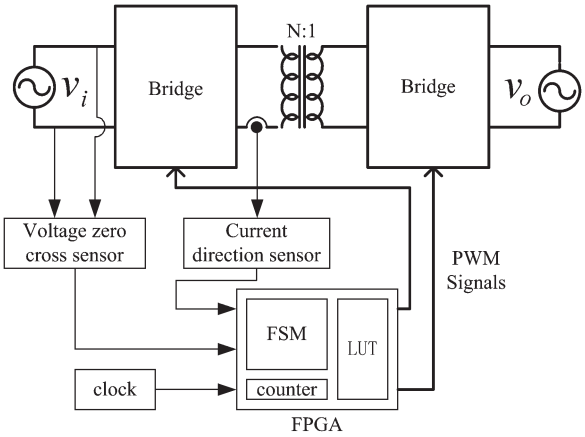

Fig. 9. Hardware diagram.

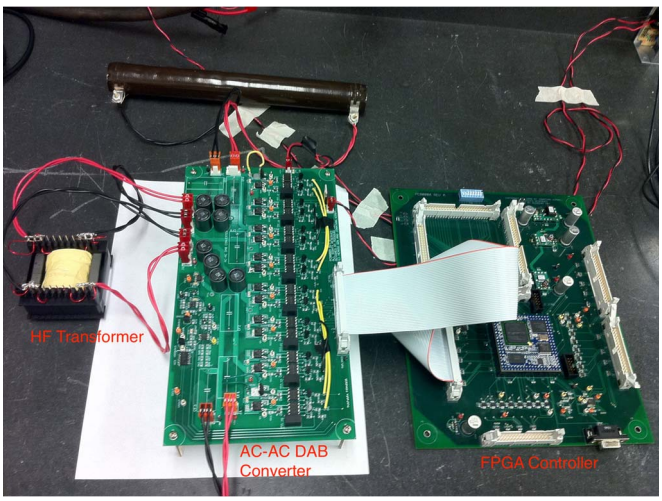

Fig. 10. Experimental prototype.

transformer design specifications, respectively. A controller for the ac–ac DAB converter was implemented in a single-chip Cyclone II field-programmable gate array from Altera. It reads input-voltage and transformer current direction signals, feeds them to a look-up table, and then sends out PWM signals. Fig. 9 shows the system diagram of the ac–ac DAB converter. A photograph of the experimental prototype is shown in Fig. 10. Experimental results are shown in Figs. 11–22. The switching frequency is 10 kHz throughout.

Figs. 11 and 12 show the waveforms of input and output voltages and currents at 1.0-pu input voltage, in forward and reversed power flow directions, respectively. Input and output currents are sinusoidal. Some harmonic content is evident due

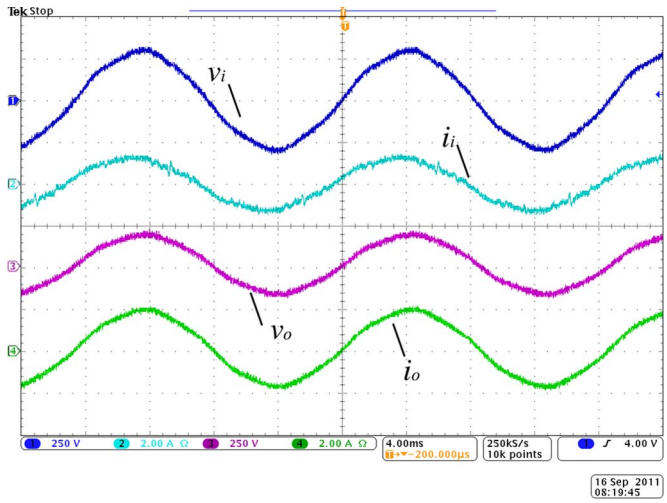

Fig. 11. Forward power flow at 1.0-pu input voltage. (From top) v_i (250 V/div), i_i (2 A/div), v_o (250 V/div), and i_o (2 A/div), 4 ms/div.

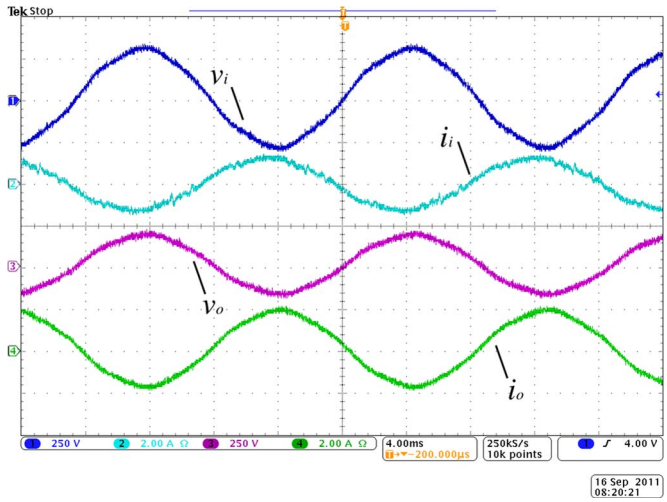

Fig. 12. Reverse power flow at 1.0-pu input voltage. (From top) v_i (250 V/div), i_i (2 A/div), v_o (250 V/div), and i_o (2 A/div), 4 ms/div.

to distortion in the source voltage, which translates directly to distortion in the currents and load voltage. Output voltage follows input voltage, with a small phase shift as predicted in (4) and the simulation results in [3].

In Fig. 12, current becomes out-of-phase of voltage because power is flowing in reversed direction. It confirms that the ac–ac DAB converter allows bidirectional power flow. Fig. 13 shows the waveforms at 0.9-pu input voltage. It confirms that an input-voltage sag can be compensated by varying the phase shift in the ac–ac DAB converter. Fig. 14 shows the output voltages at different input voltages. Test results of a Mass GI isolated transformer are provided for comparison. The Mass GI product is a commercial "transformer" that uses the circuit topology and control method of Kang *et al.* [5]. The output voltage of the Mass GI isolated transformer varies if its input voltage is changed. On the other hand, the output voltage of the proposed ac–ac DAB converter can be regulated when input voltage varies. Fig. 14 clearly indicates that the proposed ac–ac DAB converter is able to regulate output voltage and compensate variations in input voltage.

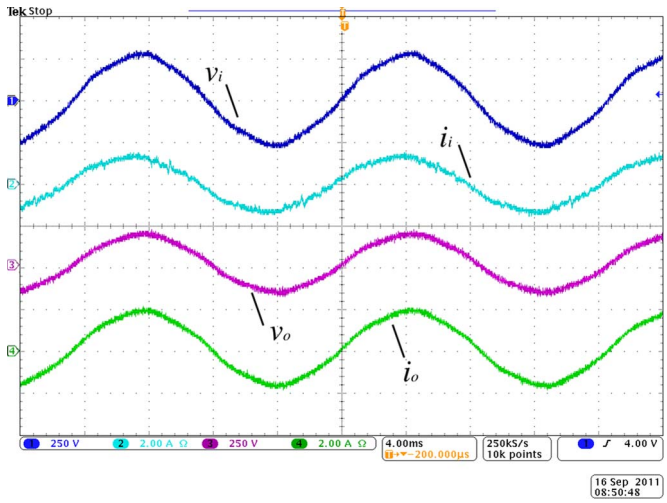

Fig. 13. Experimental waveforms at 0.9-pu input voltage. (From top) v_i (250 V/div), i_i (2 A/div), v_o (250 V/div), and i_o (2 A/div), 4 ms/div.

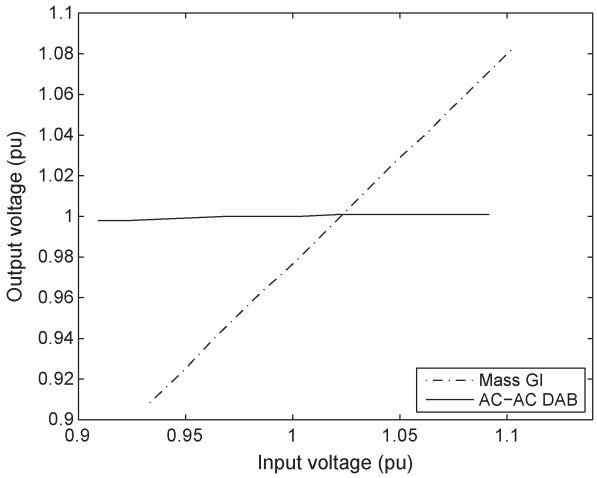

Fig. 14. Measured output voltages at different input voltages.

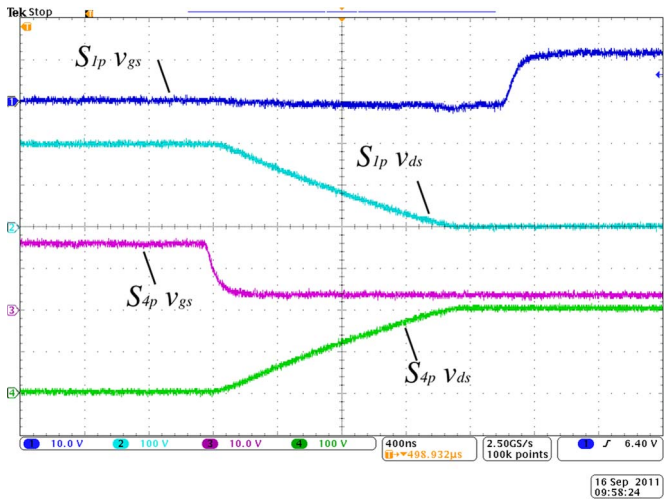

Fig. 15. Switch transient for S_{1p} and S_{4p}. (From top) $V_{\rm gs}$ (10 V/div), $V_{\rm ds}$ (100 V/div), $V_{\rm gs}$ (10 V/div), and $V_{\rm ds}$ (100 V/div), 400 ns/div.

Figs. 15 and 16 show the soft-switching transient from S_{4p} and S_{4n} to S_{1p} and S_{1n} in the first quadrant. S_{1p} is turned on after its drain-to-source voltage becomes zero. S_{4p} and S_{4n} are turned off when their drain-to-source voltages are zero. S_{1n} is turned on when its drain current is zero. The current ringing in

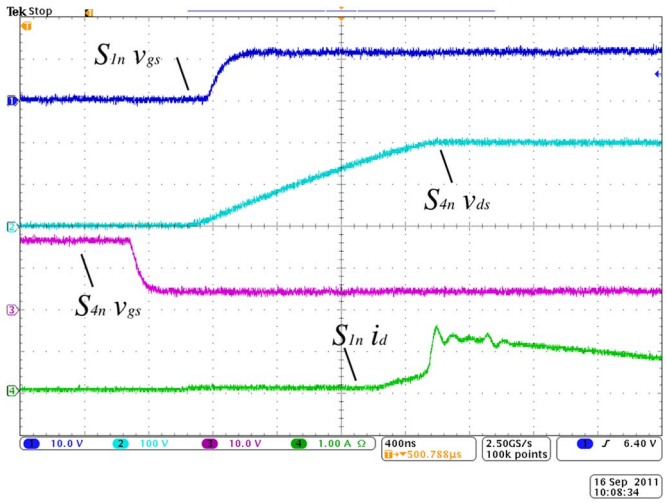

Fig. 16. Switching transient for S_{1n} and S_{4n}. (From top) $V_{\rm gs}$ (10 V/div), $V_{\rm ds}$ (100 V/div), $V_{\rm gs}$ (10 V/div), and I_d (1 A/div), 400 ns/div.

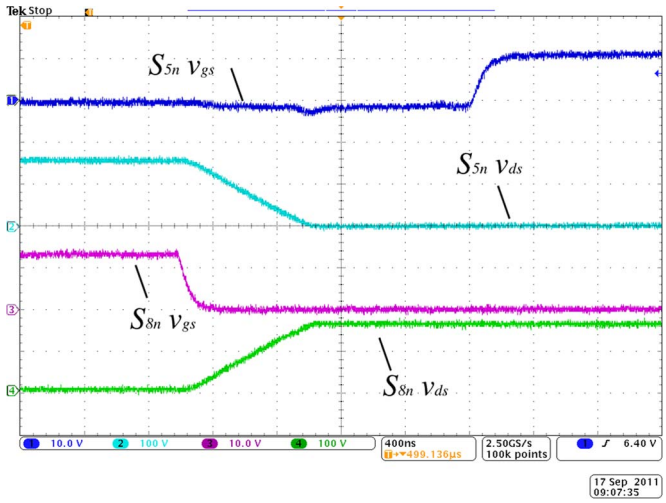

Fig. 17. Switching transient for S_{5n} and S_{8n}. (From top) $V_{\rm gs}$ (10 V/div), $V_{\rm ds}$ (100 V/div), $V_{\rm gs}$ (10 V/div), and $V_{\rm ds}$ (100 V/div), 400 ns/div.

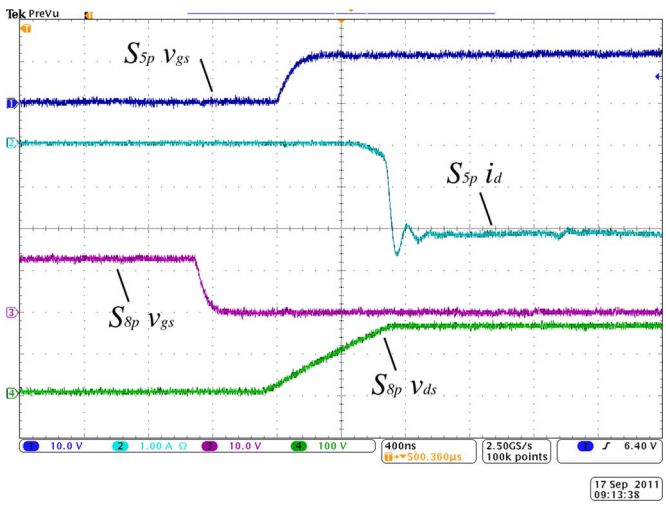

Fig. 18. Switching transient for S_{5p} and S_{8p}. (From top) $V_{\rm gs}$ (10 V/div), I_d (1 A/div), $V_{\rm gs}$ (10 V/div), and $V_{\rm ds}$ (100 V/div), 400 ns/div.

Fig. 16 is the result of body diode reverse recovery. Therefore, S_{1p}, S_{4p}, and S_{4n} switch at zero voltage, while S_{1n} switches at zero current. Figs. 17 and 18 show the soft-switching transient

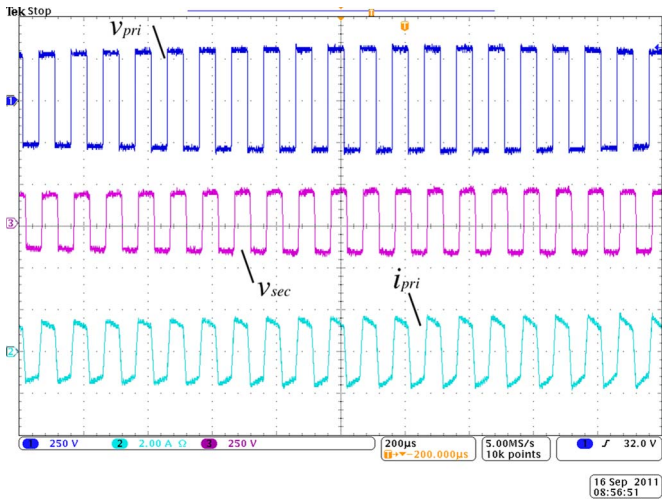

Fig. 19. Transformer waveform around peak voltage. (From top) $v_{\rm pri}$ (250 V/div), $v_{\rm sec}$ (250 V/div), and $i_{\rm pri}$ (2 A/div), 200 μs/div.

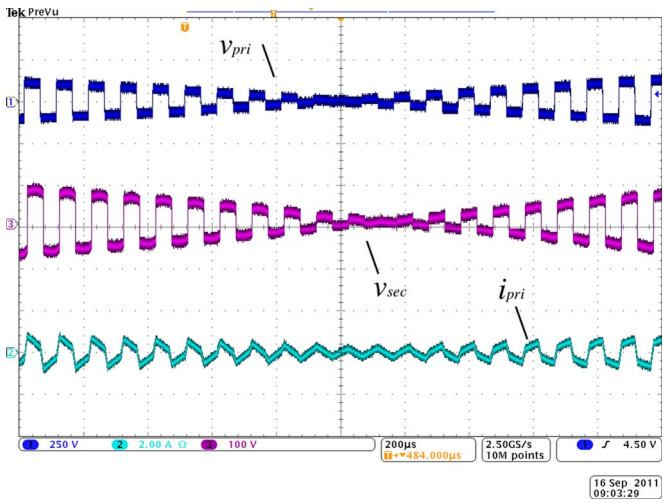

Fig. 20. Transformer waveform around zero crossing. (From top) $v_{\rm pri}$ (250 V/div), $v_{\rm sec}$ (100 V/div), and $i_{\rm pri}$ (2 A/div), 200 μs/div.

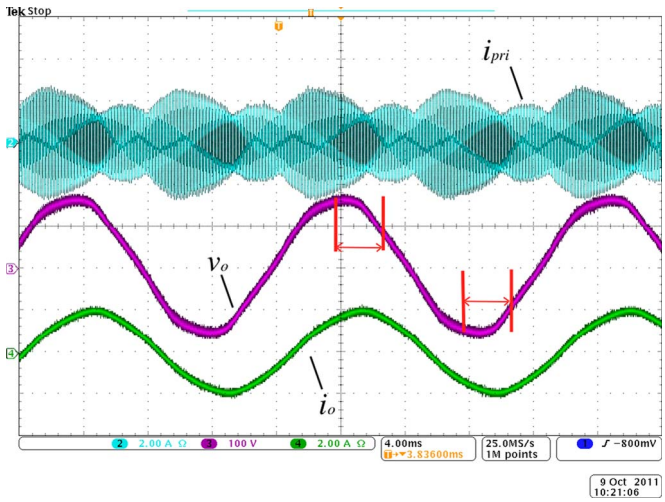

Fig. 21. Soft-switching range under a RL load. From top, $i_{\rm pri}$ (2 A/div), v_o (100 V/div), and i_o (2 A/div), 4 ms/div.

from S_{8p} and S_{8n} to S_{5p} and S_{5n} in the third quadrant. Similar results are observed at the low-voltage side. S_{5n} is turned on after its drain-to-source voltage becomes zero. S_{8p} and S_{8n} are

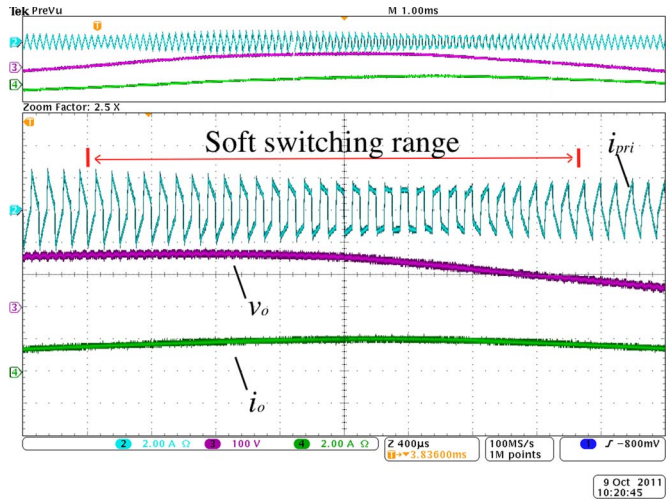

Fig. 22. Soft-switching range under a RL load (zoomed-in). From top, $i_{\rm pri}$ (2 A/div), v_o (100 V/div), and i_o (2 A/div), 400 μs/div.

turned off when their drain-to-source voltages are zero. S_{5p} is turned on when its drain current is zero. Therefore, S_{5n}, S_{8p}, and S_{8n} switch at zero voltage, while S_{5p} switches at zero current. The circuit of an ac–ac DAB converter is symmetric. Thus, soft switching is valid for other switches.

Fig. 19 shows transformer voltage and current waveforms. The direction of current permits soft switching for commutation at both primary and secondary bridges. Fig. 20 shows the transformer voltage and current around zero-crossing points. A small phase shift occurs between primary and secondary voltages, as predicted in (4). The experiment compares favorably to the simulated results shown in Figs. 6 and 7. The slight difference in transformer current slope is attributed to the extra leakage inductances in the experiment that are not included in the simulation, such as wiring and probe inductances.

Figs. 21 and 22 show the soft-switching range under RL loads. In this case, the load impedance is 1.0 pu, and its power factor is 0.86 lagging. Fig. 21 marks the soft-switching range, and Fig. 22 is a zoomed-in view of Fig. 21. The soft-switching range begins at the point in the 60-Hz cycle where the current at ϕ is positive to drive the soft-switching transients, and it ends when the current at π becomes too low to drive the soft-switching transients. The circuit is symmetric, so that the same range applies near both the positive and the negative peak. In Fig. 22, soft switching is only valid around 80°–120° during one 60-Hz period, which is consistent with the calculated result given by Fig. 2(b). This experiment verifies that the soft-switching range decreases as load power factor decreases.

Fig. 23 shows the calculated and measured efficiency of a prototype ac–ac DAB converter. Efficiency calculation was based on the loss evaluation methods discussed in [14], and efficiency measurement was performed by measuring input voltage/current and output voltage/current. The measured results are consistent with the calculated ones. Efficiency is high around rated power because of soft switching. However, efficiency drops significantly when power is less than 30%. The reasons for low efficiency at light load are: 1) soft switching is not available at light load and 2) the transformer loss becomes more significant at light load. Higher efficiency is necessary to

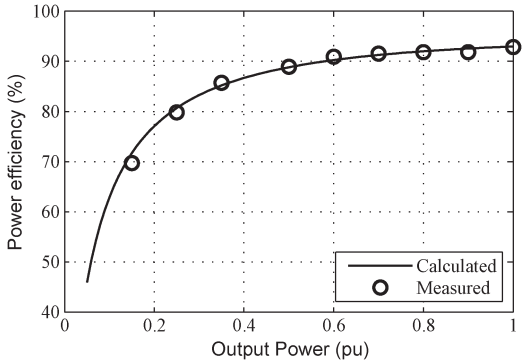

Fig. 23. Calculated and measured power efficiency.

compete with traditional transformers, which requires overall converter design optimization [37] and, possibly, a new switching strategy [42].

VI. Conclusion and Future Work

This paper has presented a novel ac–ac DAB converter for SSTs. A high-frequency transformer is used to minimize the bulk of passive components. Four-quadrant switch cells and PSM ensure that energy can flow in both directions. Operating modes and soft-switching conditions have been analyzed in detail using a generalized per-unit model. Soft switching is valid over a wide range of load and voltage variations. A switching commutation method is developed for both soft and hard switching. Experimental results confirm that the proposed ac–ac DAB converter can provide a regulated output voltage when the input voltage varies.

This paper presents a proof-of-concept study of applying ac–ac DAB converters as SSTs. Several challenges remain for the success of SSTs: 1) the availability of SiC-based high-voltage high-frequency switching device to support operation at distribution voltages; 2) hardware optimization and control strategy to improve low power efficiency; 3) closed-loop controller to compensate steady-state phase shift and grid disturbance; and 4) achieving high-voltage isolation (input-to-output, phase-to-ground) without significant cost or performance penalties and with adequate electromagnetic compatibility (EMC). These will be investigated in future works. Closed-loop control can benefit from a model similar to that in [40], adapted to the ac–ac case. EMC requires careful attention to the transformer design and construction [43] but benefits from the soft switching inherent to the proposed DAB topology. Other SST topologies face similar challenges, plus additional difficulties (such as interaction between stages in a multistage topology) or expenses (such as high-voltage capacitors).

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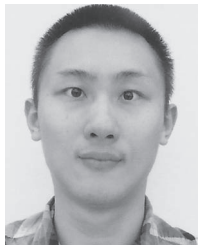

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